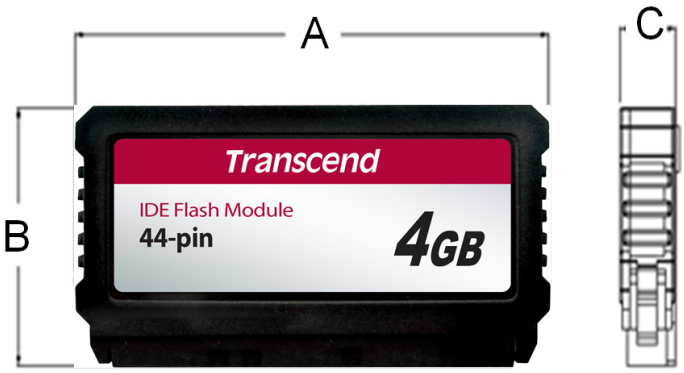
44-Pin IDE Flash Module (Vertical)

Description

With an IDE interface and strong data retention ability, 44-Pin IDE Flash Modules are ideal for use in harsh environments where Industrial PCs, Set-Top Boxes, etc. are used.

Placement



Dimensions

Side	Millimeters	Inches
A	52.00 ± 0.40	2.047 ± 0.016
B	29.5 ± 0.50	1.162 ± 0.020
C	7.20 ± 0.20	0.284 ± 0.008

Features

- RoHS compliant
- Power supply: 3.3V±5% or 5V±10%
- Operating temperature: 0°C to 70°C
- Storage temperature: -40°C to 85°C
- Humidity (Non condensation): 0% to 95%
- Built-in 72 bit per 1K Byte ECC (Error Correction Code) functionality to ensure high reliability of data transfer
- Global wear-leveling algorithm to eliminate excessive write operation and extend product life
- Supports S.M.A.R.T (Self-defined)
- Supports Security Command
- Supports Host Protected Area
- Supports Ultra DMA Mode 0 to 5
- Supports Multiword DMA Mode 0 to 2
- Supports PIO Mode 0 to 4
- Durability of connector: 100 times
- MTBF: 1,000,000 hours (in 25°C)

■ Specifications

Physical Specification		
Form Factor		
Storage Capacity		128 MB to 4 GB
Dimensions (mm)	**Length**	52.00 ± 0.40
	Width	29.50 ± 0.50
	Height	7.20 ± 0.20
Input Voltage		3.3V ± 5% or 5V ± 10%
Connector		44 pin IDE female connector

Environmental Specifications		
Operating Temperature		0 ℃ to 70 ℃
Storage Temperature		- 40 ℃ to 85 ℃
Humidity	**Operating**	0% to 95% (Non-condensing)
	Non-Operating	0% to 95% (Non-condensing)

Reliability	
Data Reliability	Supports BCH ECC 72 bit per 1K byte
Connector Durability	100 times
MTBF	1,000,000 hours
TBW	TBT

Regulations	
Compliance	CE, FCC and BSMI

Performance				
Model P/N	**Read**	**Write**	**Random Read** (4KB QD32)	**Random Write** (4KB QD32)
TS128MPTM720	39.40 MB/s	8.615 MB/s	10.60 MB/s	0.178 MB/s
TS256MPTM720	39.40 MB/s	8.615 MB/s	10.60 MB/s	0.178 MB/s
TS512MPTM720	20.79 MB/s	7.637 MB/s	8.139 MB/s	0.338 MB/s
TS1GPTM720	20.85 MB/s	13.75 MB/s	6.382 MB/s	0.237 MB/s

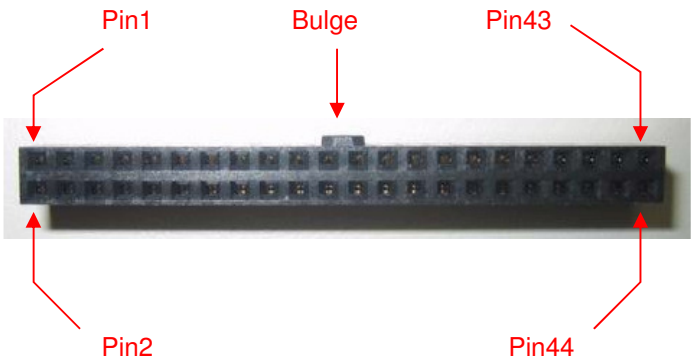
Note: 25 °C, test on GA-Z87-UD3H-CF, 4GB RAM, Windows® 8.1 with AHCI mode, benchmark utility Crystal Disk Mark (version 3.0), copied file 1000MB.

Actual Capacity				
Model P/N	**User Max. LBA**	**Cylinder**	**Head**	**Sector**
TS128MPTM720	249,984	248	16	63
TS256MPTM720	499,968	496	16	63
TS512MPTM720	1,000,944	993	16	63
TS1GPTM720	1,957,536	1,942	16	63

■ Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
01	RESET#	12	HD12	23	IOWB	34	PDIAGB
02	GND	13	HD2	24	GND	35	HA0
03	HD7	14	HD13	25	IORB	36	HA2
04	HD8	15	HD1	26	GND	37	CE1B
05	HD6	16	HD14	27	IORDY	38	CE2B
06	HD9	17	HD0	28	NC	39	DASPB
07	HD5	18	HD15	29	DMACK#	40	GND
08	HD10	19	GND	30	GND	41	VCC
09	HD4	20	VCC	31	IREQ	42	VCC
10	HD11	21	DMARQ	32	IOIS16B	43	GND
11	HD3	22	GND	33	HA1	44	GND

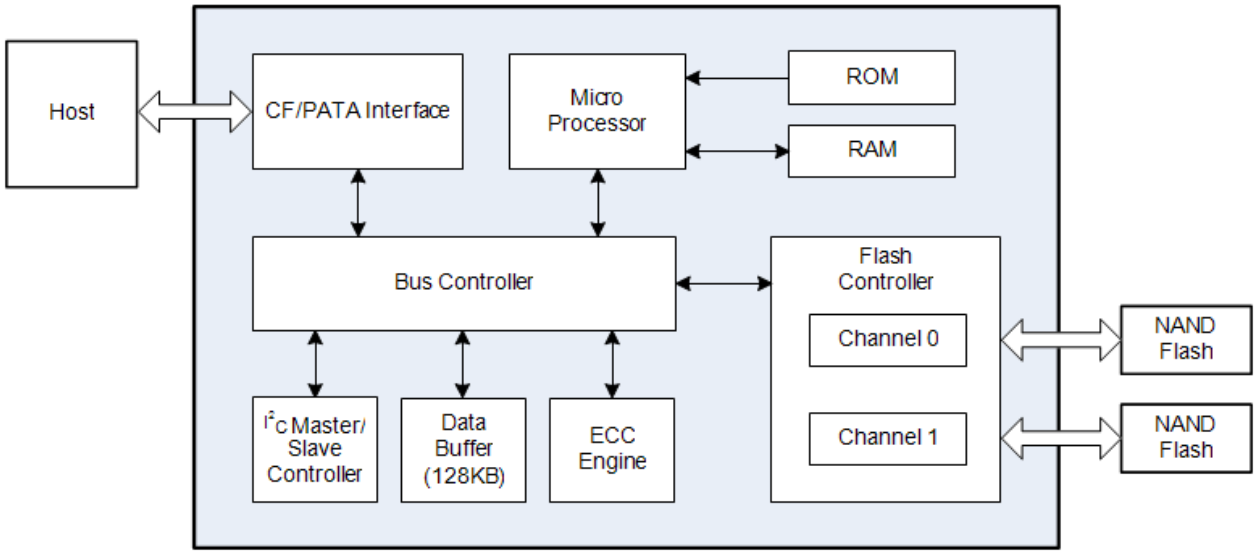
■ Pin Layout

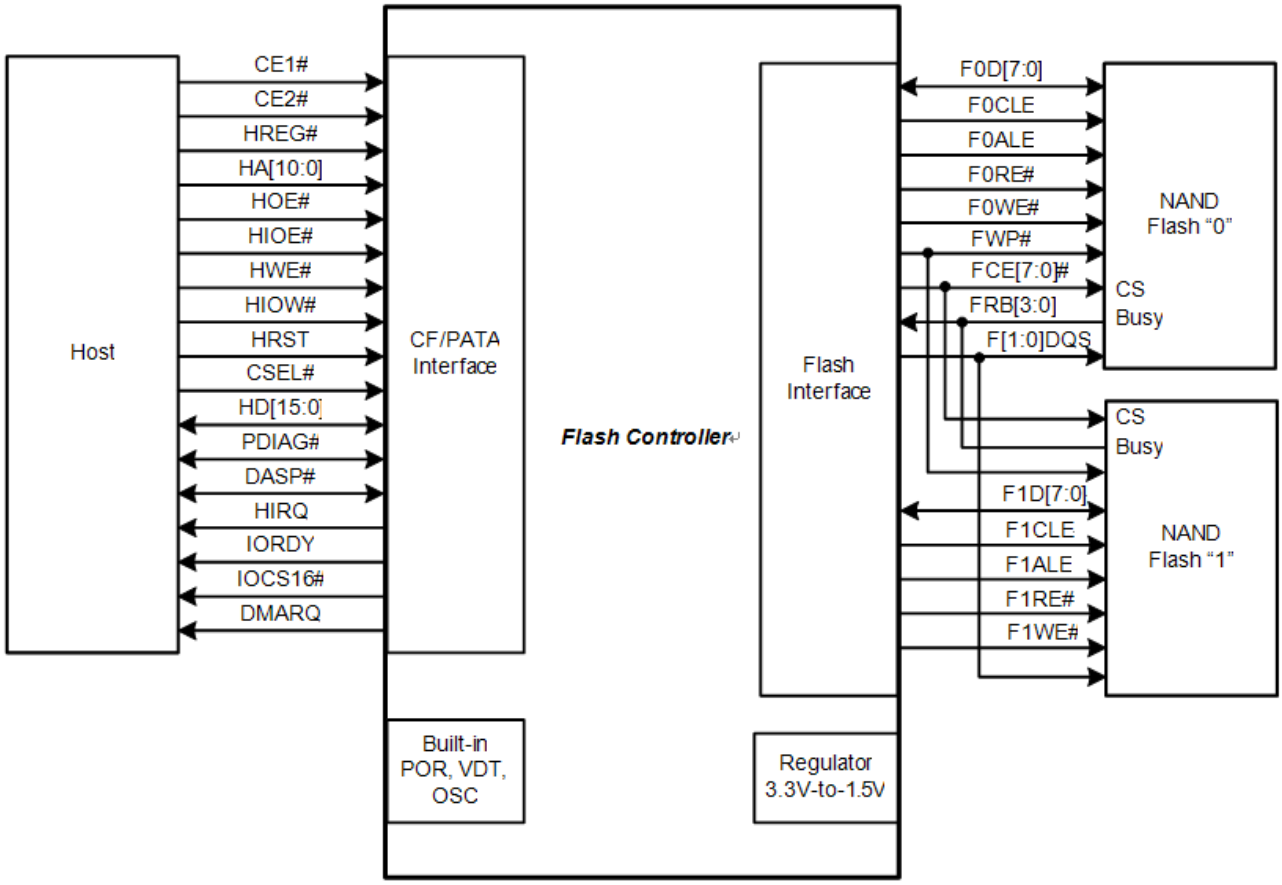


■ Pin Definition

Symbol	Function
HD0 ~ HD15	Data Bus (Bi-directional)
HA0 ~ HA2	Address Bus (Input)
RESET#	Device Reset (Input)
IORB	Device I/O Read (Input)
IOWB	Device I/O Write (Input)
IOIS16B	Transfer Type 8/16 bit (Output)
CE1B, CE2B	Chip Select (Input)
PDIAGB	Pass Diagnostic (Bi-directional)
DASPB	Disk Active/Slave Present (Bi-directional)
DMARQ	DMA request
DMACK#	DMA acknowledge
IREQ	Interrupt Request (Output)
NC	No Connection
GND	Ground
VCC	Vcc Power Input

■ Block Diagram





■ Reliability

Global Wear Leveling – Advanced algorithm to enhance the Wear-Leveling Efficiency

Global wear leveling ensures every block has an even erase count. By ensuring all spare blocks in the SSD’s flash chips are managed in a single pool, each block can then have an even erase count. This helps to extend the lifespan of a SSD and to provide the best possible endurance.

There are three main processes in global wear -leveling:

- Record the block erase count and save this in the wear-leveling table.
- Finds the static-block and saves this in the wear-leveling pointer.

Checks the erase count when a block is pulled from the pool of spare blocks. If the erased block count is larger than the Wear Count (WEARCNT), then the static blocks are leveraged against the over-count blocks.

StaticDataRefresh Technology – Keeping Data Healthy

Many variants may disturb the charge inside a Flash cell. These variants can be: time, read operations, undesired charge, heat, etc. Each variant would create a charge loss, which slightly influences the charge levels. In our everyday usage, more than 60% are repeated read operations, and the accumulated charge loss would eventually result in the data loss. Normally, the ECC engine corrections take place without affecting normal host operations. Over time, the number of bit errors accumulated in the read transaction exceeds the correcting capacity of the ECC engine, which results in corrupted data being sent to the host. To prevent this, the controller monitors the bit error levels during each read operation; when the number of bit errors reaches the preset threshold value, the controller automatically performs a data refresh to “restore” the correct charge levels in the cell. Implementation of StaticDataRefresh Technology reinstates the data to its original, error-free state, and hence, lengths the data’s lifespan.

EarlyRetirement – Avoiding Data Loss Due to Weak Block

The StaticDataRefresh feature functions well when the cells in a block are still healthy. As the block ages over time, it cannot store charge reliably anymore, EarlyRetirement enters the scene. EarlyRetirement works by moving the static data to another block (a health block) before the previously used block becomes completely incapable of holding charges for data. When the charge loss error level exceeds another threshold value (higher from that for StaticDataRefresh), the controller automatically moves its data to another block. In addition, the original block is then marked as a bad block, which prevents its further use, and thus the block enters the state of “EarlyRetirement.” Note that, through this process, the incorrect data are detected and effectively corrected by the ECC engine, thus the data in the new block is stored error-free.

Advanced Power Shield – Avoiding Data Loss during Power Failure

When a power failure takes place, the line voltage drops. When it reaches the first Logic-Freeze Threshold, the core controller is held at a steady state. Here are some implications: Firstly, it ceases the communication with the host. This prevents the host from sending in further address/instructions/data that may be corrupted. During power disturbance, the host is likely experiencing a voltage drop, so the transmission integrity cannot be guaranteed. Secondly, it stops sending the information to the Flash, which prevents the controller from corrupting the address/data being transmitted to the Flash, and corrupting the Flash contents inadvertently. Furthermore, Advanced Power Shield cuts off the connection of host power and turns off the controller to reserve most of the energy for NAND Flash to complete programming. Owing to the SLC structure, an interrupted programming may damage a paired page and cause the loss of the previously written data.

■ Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD-VSS	DC Power Supply	-0.6	+6	V
Ta	Operating Temperature	0	70	°C
Tst	Storage Temperature	-40	+85	°C

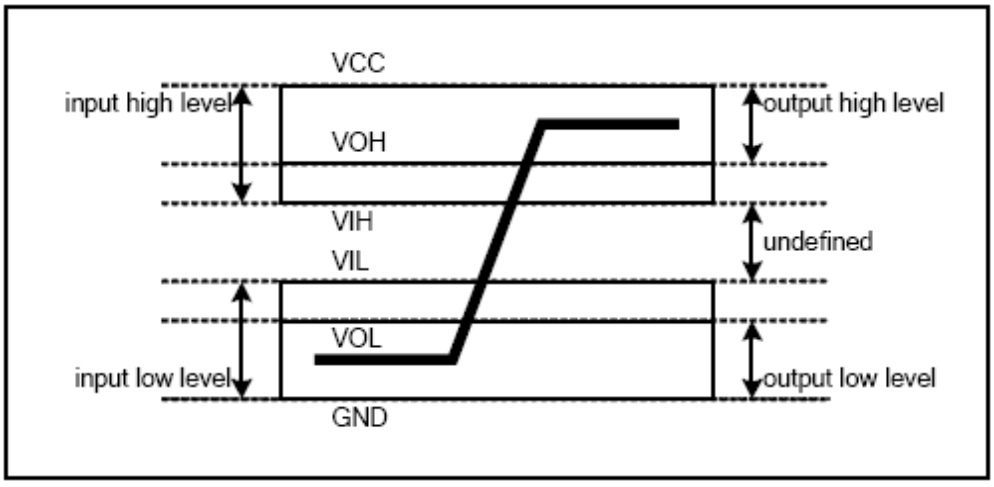
■ Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
VDD	Power supply	3.0	5.5	V
VIN	Input voltage	0	VDD+0.3	V
Ta	Operating Temperature	0	+70	°C

■ DC Characteristics

(Ta=0 °C to +70 °C, Vcc = 3.3V ±5% or 5.0V ±10%)

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage 5V	VCC	4.5	5.5	V	
Supply Voltage 3.3V	VCC	2.97	3.63	V	
High level output voltage	VOH	2.5	--	V	
Low level output voltage	VOL	--	0.4	V	
High level input voltage	VIH	2.4	--	V	Non-schmitt trigger
		2.05	--	V	Schmitt trigger[1]
Low level input voltage	VIL	--	0.6	V	Non-schmitt trigger
		--	1.25	V	Schmitt trigger[1]

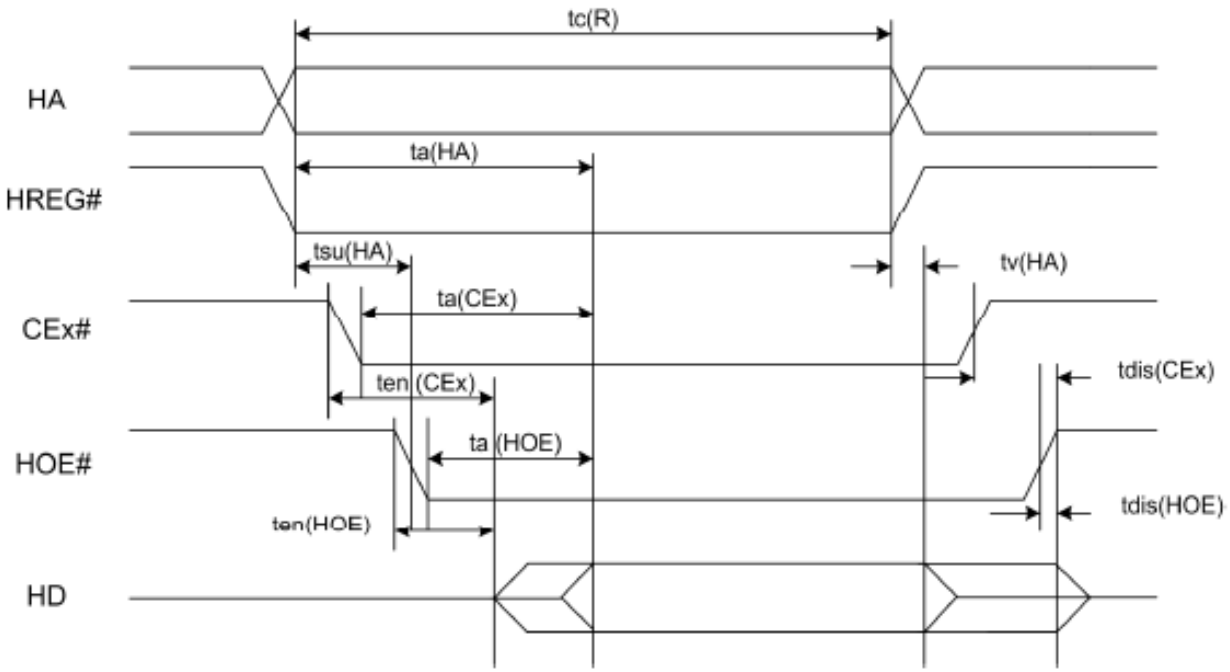


■ Attribute Memory Read Timing Specification

Attribute Memory access time is defined as 300 ns. Detailed timing specs are shown in the Table below

Speed Version			300 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

Note: All time intervals are recorded in nanoseconds. HD refers to data provided by the CompactFlash Storage Card to the system. The CEx# signal or both the HOE# and the HWE# signals are reasserted between consecutive cycle operations.



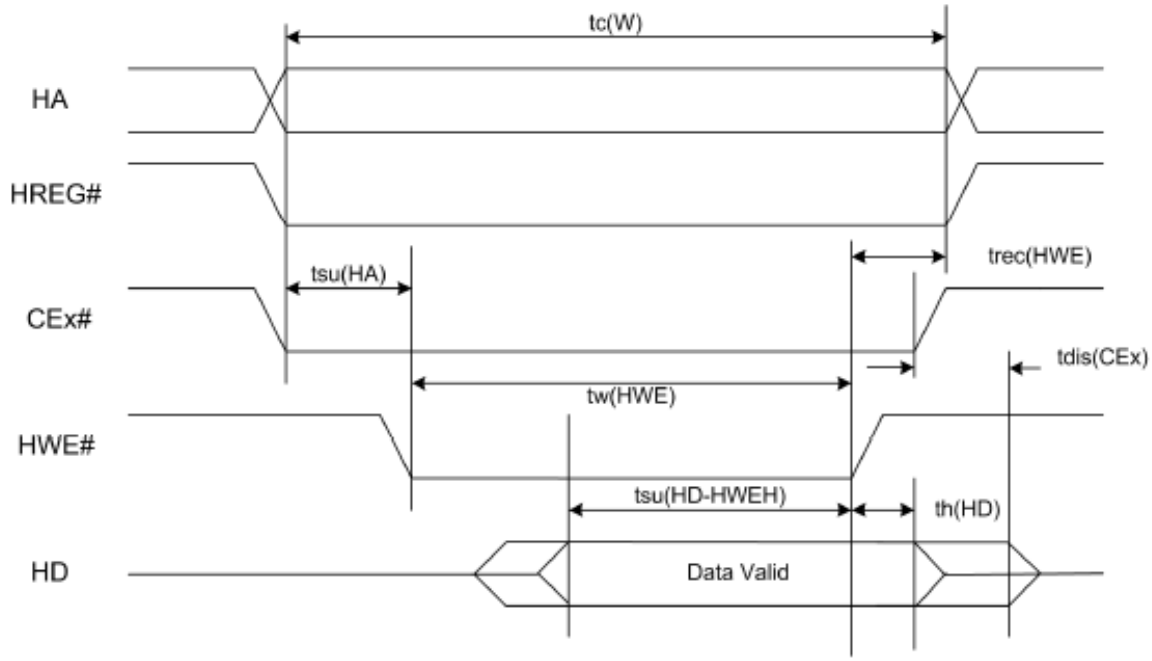
■ Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250 ns. Detailed timing specifications are shown in the Table below.

Table: Configuration Register (Attribute Memory) Write Timing

Speed Version		250 ns	
Item	**Symbol**	**Min ns**	**Max ns**
Write Cycle Time	tc(W)	250	
Write Pulse Width	tw(HWE)	150	
Address Setup Time	tsu(HA)	30	
Write Recovery Time	trec(HWE)	30	
Data Setup Time for WE	tsu(HD-HWEH)	80	
Data Hold Time	th(HD)	30	

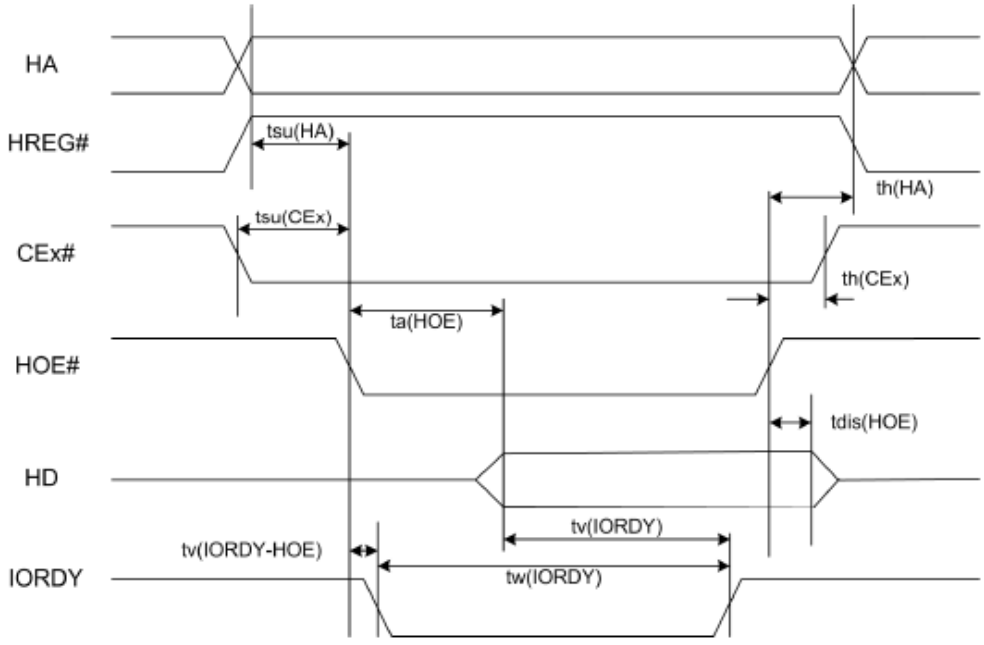
Note: All time intervals are recorded in nanoseconds. HD refers to data provided by the system the CompactFlash Card.



■ Common Memory Read Timing Specification

		Cycle Time Mode:	250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Output Enable Access Time	ta(HOE)	tGLQV		125		60		50		45
Output Disable Time from HOE	tdis(HOE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(HA)	tAVGL	30		15		10		10	
Address Hold Time	th(HA)	tGHAX	20		15		15		10	
CEx Setup before HOE	tsu(CEx)	tELGL	5		5		5		5	
CEx Hold following HOE	th(CEx)	tGHEH	20		15		15		10	
Wait Delay Falling from HOE	tv(IORDY-HOE)	tGLWTV		35		35		35		na[1]
Data Setup for Wait Release	tv(IORDY)	tQVWTH		0		0		0		na[1]
Wait Width Time[2]	tw(IORDY)	tWTLWTH		350		350		350		na[1]

Notes:
1) IORDY is not supported in this mode.
2) The maximum load on IORDY is 1 LSTTL with 50 pF (40pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. HD refers to data provided by the CompactFlash Storage Card to the system. The IORDY signal can be ignored when the HOE# cycle-to-cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure (CIS). Although adhering to the PCMCIA specification of 12µs, the Wait Width time is intentionally lower in this specification.

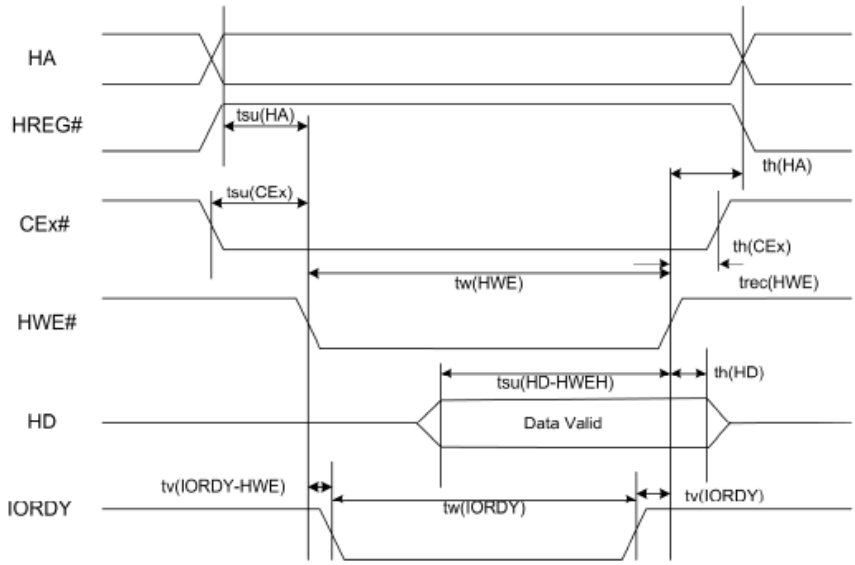


■ Common Memory Write Timing Specification

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before HWE	tsu (HD-HWEH)	tDVWH	80		50		40		30	
Data Hold following HWE	th(HD)	tWMDX	30		15		10		10	
HWE Pulse Width	tw(HWE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(HA)	tAVWL	30		15		10		10	
CEx Setup before HWE	tsu(CEx)	tELWL	5		5		5		5	
Write Recovery Time	trec(HWE)	tWMAX	30		15		15		15	
Address Hold Time	th(HA)	tGHAX	20		15		15		15	
CEx Hold following HWE	th(CEx)	tGHEH	20		15		15		10	
Wait Delay Falling from HWE	tv (IORDY-HWE)	tWLWTV		35		35		35		na[1]
WE High from Wait Release	tv(IORDY)	tWTHWH	0		0		0		na[1]	
Wait Width Time[2]	tw (IORDY)	tWTLWTH		350		350		350		na[1]

Notes:

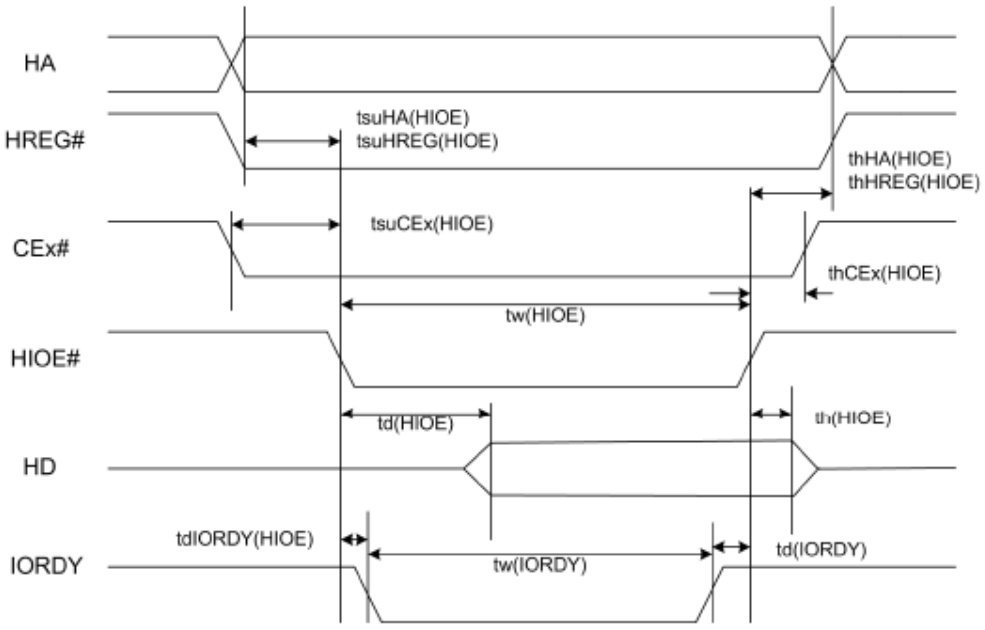
1) IORDY is not supported in this mode.
2) The maximum load on IORDY is 1 LSTTL with 50 pF (40pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. HD refers to data provided by the CompactFlash Storage Card to the system. The IORDY signal can be ignored when the HOE# cycle-to-cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure (CIS). Although adhering to the PCMCIA specification of 12µs, the Wait Width time is intentionally lower in this specification.



■ I/O Input (Read) Timing Specification

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Delay after HIOE	td(HIOE)	tIGLQV		100		50		50		45
Data Hold following HIOE	th(HIOE)	tIGHQX	0		5		5		5	
HIOE Width Time	tw(HIOE)	tIGLIGH	165		70		65		55	
Address Setup before HIOE	tsuA(HIOE)	tAVIGL	70		25		25		15	
Address Hold following HIOE	thA(HIOE)	tIGHAX	20		10		10		10	
CEx Setup before HIOE	tsuCE(HIOE)	tELIGL	5		5		5		5	
CEx Hold following HIOE	thCE(HIOE)	tIGHEH	20		10		10		10	
HREG Setup before HIOE	tsuREG (HIOE)	tRGLIGL	5		5		5		5	
HREG Hold following HIOE	thREG (HIOE)	tIGHRGH	0		0		0		0	
Wait Delay Falling from HIOE[2]	tdWT(HIOE)	tIGLWTL		35		35		35		Na[1]
Data Delay from Wait Rising[2]	td(IORDY)	tWTHQV		0		0		0		Na[1]
Wait Width Time[2]	tw(IORDY)	tWTLWTH		350		350		350		Na[1]

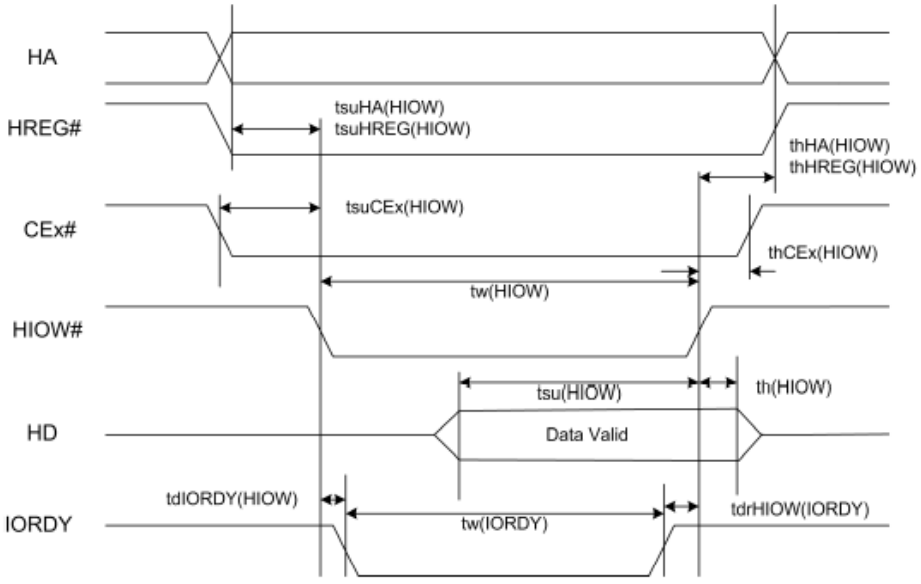
Notes:
1) IORDY is not supported in this mode.
2) The maximum load on IORDY is 1 LSTTL with 50 pF (40pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met. HD refers to data provided by the CompactFlash Storage Card to the system. Although adhering to the PCMCIA specification of 12µs, the Wait Width time is intentionally lower in this specification.



I/O Output (Write) Timing Specification

Cycle Time Mode:			255 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before HIOW	tsu(HIOW)	tDVIWH	60		20		20		15	
Data Hold following HIOW	th(HIOW)	tIWHDX	30		10		5		5	
HIOW Width Time	tw(HIOW)	tIWLIWH	165		70		65		55	
Address Setup before HIOW	tsuA(HIOW)	tAVIWL	70		25		25		15	
Address Hold following HIOW	thA(HIOW)	tIWHAX	20		20		10		10	
CEx Setup before HIOW	tsuCE (HIOW)	tELIWL	5		5		5		5	
CEx Hold following HIOW	thCE (HIOW)	tIWHEH	20		20		10		10	
HREG Setup before HIOW	tsuREG (HIOW)	tRGLIWL	5		5		5		5	
HREG Hold following HIOW	thREG (HIOW)	tIWHRGH	0		0		0		0	
Wait Delay Falling from HIOW[2]	tdWT(HIOW)	tIWLWTL		35		35		35		Na[1]
HIOW high from Wait high[2]	tdrHIOW (IORDY)	tWTJIWH	0		0		0		Na[1]	
Wait Width Time[2]	tw(IORDY)	tWTLWTH		350		350		350		Na[1]

Notes:
1) IORDY is not supported in this mode.
2) The maximum load on IORDY is 1 LSTTL with 50 pF (40pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met. HD refers to data provided by the CompactFlash Storage Card to the system. Although adhering to the PCMCIA specification of 12µs, the Wait Width time is intentionally lower in this specification.



■ True IDE PIO Mode Read/Write Timing Specification

	Item	Mode							Note
		0	1	2	3	4	5	6	
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to HIOE/HIOW setup (min)	70	50	30	30	25	15	10	
t2	HIOE/HIOW (min)	165	125	100	80	70	65	55	1
t2	HIOE/HIOW (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	HIOE/HIOW recovery time (min)	-	-	-	70	25	25	20	1
t3	HIOW data setup (min)	60	45	30	30	20	20	15	
t4	HIOW data hold (min)	30	20	15	10	10	5	5	
t5	HIOE data setup (min)	50	35	20	20	20	15	10	
t6	HIOE data hold (min)	5	5	5	5	5	5	5	
T6Z	HIOE data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	HIOE/HIOW to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na[5]	na[5]	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na[5]	na[5]	
tC	IORDY assertion to release (max)	5	5	5	5	5	na[5]	na[5]	

Notes:

All timings are in nanoseconds. The maximum load on IOCS16# is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met.

1) Where t0 denotes the minimum total cycle time; t2 represents the minimum command active time; t2i is the minimum command recovery time or command inactive time. Actual cycle time equals the sum of actual command active time and actual command inactive time. The three timing requirements for t0, t2, and t2i are met. The minimum total cycle time requirement is greater than the sum of t2 and t2i, implying that a host implementation can extend either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identity data. A CompactFlash Card implementation supports any legal host implementation.

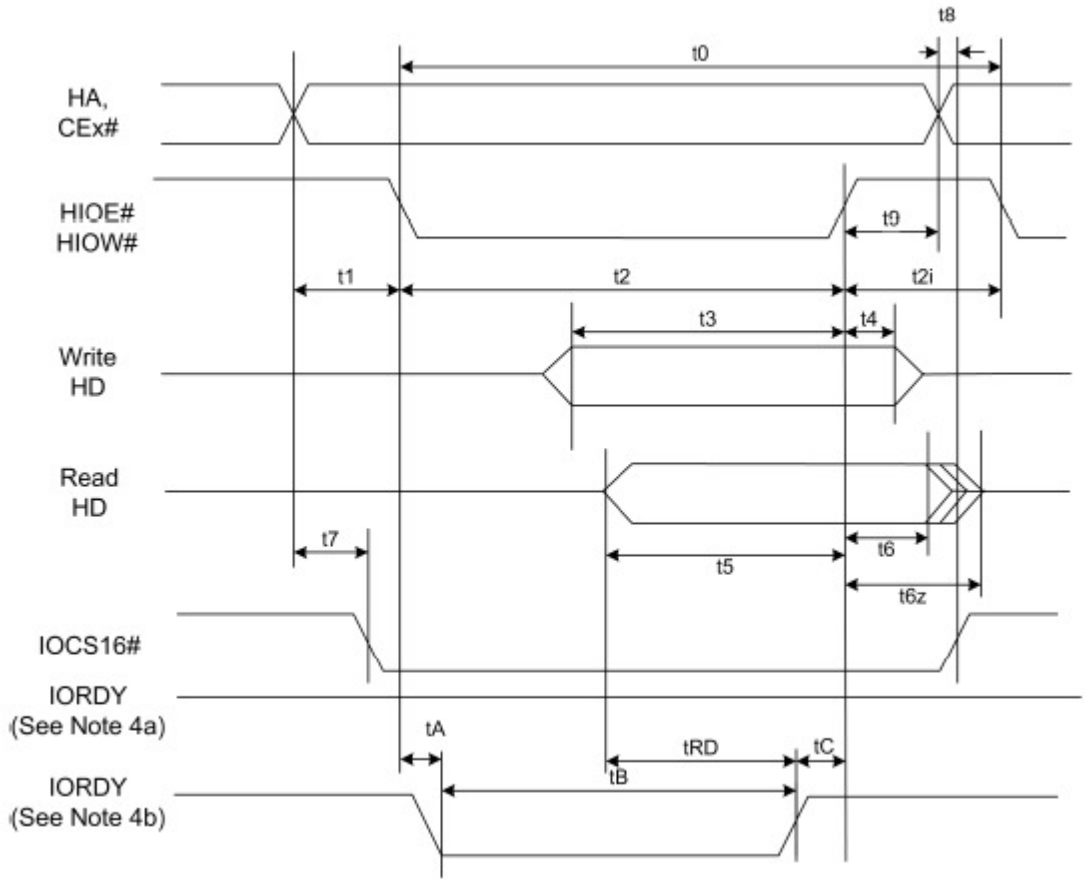
2) This parameter specifies the time from the negation edge of the HIOE# to the time that the CompactFlash Card (tri-state) no longer drives the data bus.

3) The delay originates from HIOE# or HIOW# activation until the state of IORDY is first sampled. If IORDY is inactive, the host waits until IORDY is active before the PIO cycle is completed. When the CompactFlash Storage Card is not driving IORDY, which is negated at tA after HIOE# or HIOW# activation, then t5 is met and tRD is inapplicable. When the

CompactFlash Card is driving IORDY, which is negated at the time tA after HIOE# or HIOW# activation, then tRD is met and t5 is inapplicable.

4) Both t7 and t8 apply to modes 0, 1, and 2 only. For other modes, this signal is invalid.

5) IORDY is not supported in this mode.



Notes:

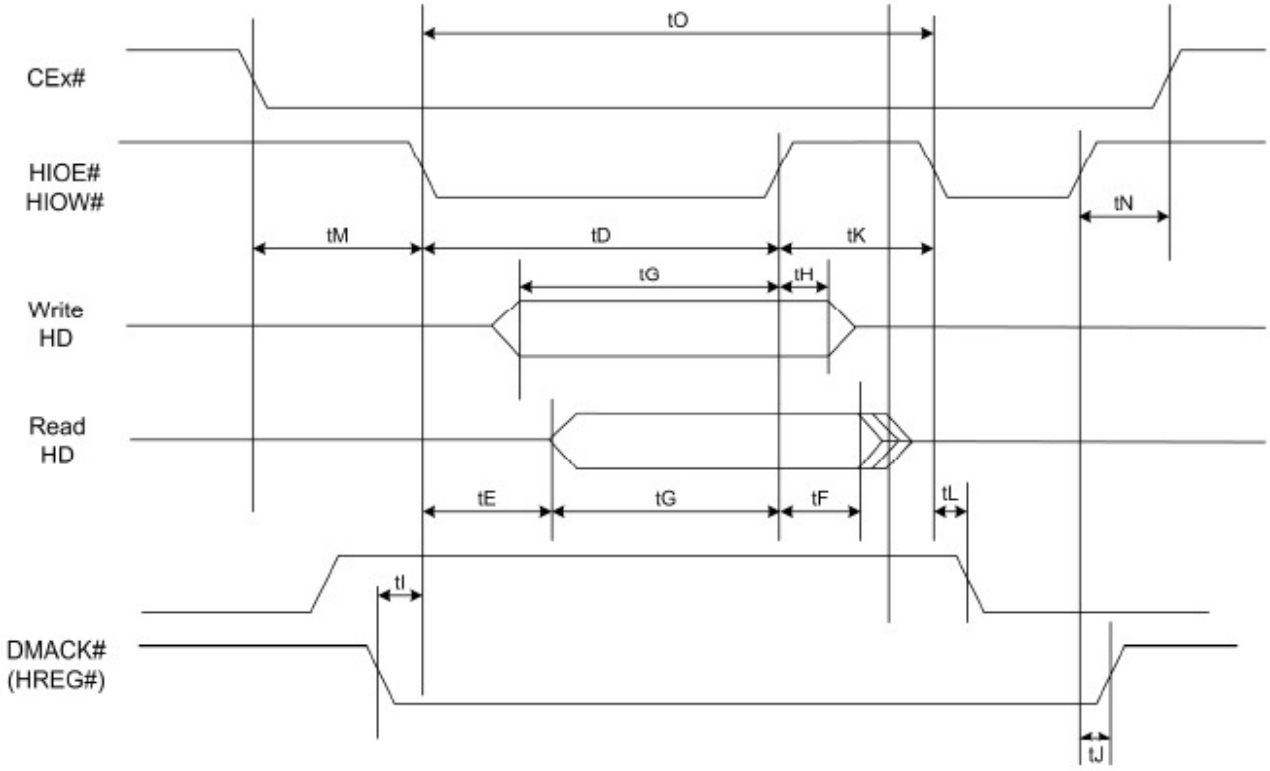
1) Device address comprises CE1#, CE2#, and HA[2:0].
2) Data comprises HD[15:0] (16-bit) or HD[7:0] (8-bit).
3) IOCS16# is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.
4) The negation of IORDY by the device is used to lengthen the PIO cycle. Whether the cycle is to be extended is determined by the host after tA from the assertion of HIOE# or HIOW#. The assertion and negation of IORDY is described in the following three cases.
   (a) The device never negates IORDY: No wait is generated.
   (b) Device drives IORDY low before tA: a wait is generated. The cycle is completed after IORDY is reasserted.
   For cycles in which a wait is generated and HIOE# is asserted, the device places read data on D15-D00 for tRD before IORDY is asserted.

True IDE Multiword DMA Mode Read/Write Timing Specification

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	Note
t_O	Cycle time (min)	480	150	120	100	80	1
t_D	-HIOE / -HIOW asserted width (min)	215	80	70	65	55	1
t_E	-HIOE data access (max)	150	60	50	50	45	
t_F	-HIOE data hold (min)	5	5	5	5	5	
t_G	-HIOE/-HIOW data setup (min)	100	30	20	15	10	
t_H	-HIOW data hold (min)	20	15	10	5	5	
t_I	-HREG to –HIOE/-HIOW setup (min)	0	0	0	0	0	
t_J	-HIOE / -HIOW to -HREG hold (min)	20	5	5	5	5	
t_{KR}	-HIOE negated width (min)	50	50	25	25	20	1
t_{KW}	-HIOW negated width (min)	215	50	25	25	20	1
t_{LR}	-HIOE to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	-HIOW to DMARQ delay (max)	40	40	35	35	35	
t_M	CEx valid to –HIOE / -HIOW	50	30	25	10	5	
t_N	CEx hold	15	10	10	10	10	

Notes:

1) Where t0 is the minimum total cycle time and tD is minimum command active time, whereas tKR and tKW are minimum command recovery time or command inactive time for input and output cycles, respectively. Actual cycle time equals the sum of actual command active time and actual command inactive time. The three timing requirements of t0, i.e. tD, tKR, and tKW, must be met. The minimum total cycle time requirement exceeds the sum of tD and tKR or tKW for input and output cycles, respectively, implying that a host implementation can extend either or both tD and tKR or tKW as deemed necessary to ensure that t0 equals or exceeds the value reported in the device's identity data. A CompactFlash Card implementation supports any legal host implementation.



Notes:

1) If a card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ during the time from the start of a DMA transfer cycle (to suspend DMA transfers in progress) and reassertion of the signal at a relatively later time to continue DMA transfer operations.
2) The host may negate this signal to suspend the DMA transfer in progress.

■ True IDE Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		UDMA Mode 5		UDMA Mode 6		UDMA Mode 7		Measure Location (see Note[2])
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		40		30		24		Sender
t_{CYC}	112		73		54		39		25		16.8		13.0		10		Note[3]
t_{2CYC}	230		153		115		86		57		38		29		23		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		2.6		2.5		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		3.5		2.9		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		4.0		2.9		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		4.0		3.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		10.0		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		10.0		10.0		Host
t_{ZFS}	0		0		0		0		0		35		25		15.0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		17.5		10.5		Sender
t_{FS}		230		200		170		130		120		90		80		70	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	0	60		50	Note[4]
t_{MLI}	20		20		20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10		10		10	Note[5]
t_{ZAH}	20		20		20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	20	50	20	50	Host
t_{RFS}		75		70		60		60		60		50		50		50	Sender
t_{RP}	160		125		100		100		100		85		85		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		50		50		Sender

Notes:
1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and –DMARDY transitions are measured at the sender connector.
3) The parameter tCYC shall be measured at the recipient's connector farthest from the sender.
4) The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the

recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5) The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus for a bus turnaround.

■ Ultra DMA Data Burst Timing Descriptions Name Comment Note

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	6
t_{ZIORDY}	Minimum time before driving IORDY	4, 6
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

1) The parameters tUI, tMLI : (Ultra DMA Data-In Burst Device Termination Timing and Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum.
2) 80-conductor cabling shall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2.
3) Timing for tDVS, tDVH, tCVS and tCVH shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
4) For all modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- giving it a known state when released.
5) The parameters tDS and tDH for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for tDS and tDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

■ Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode4 (ns)		UDMA Mode 5 (ns)		UDMA Mode 6 (ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	14.7		9.7		6.8		6.8		4.8		2.3		2.3	
t_{DHIC}	4.8		4.8		4.8		4.8		4.8		2.8		2.8	
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5		6.0		5.2	
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0		6.0		5.2	
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)													
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)													
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)													
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)													

Notes:

1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).
3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

■ Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
SRISE	Rising Edge Slew Rate for any signal		1.25	1
SFALL	Falling Edge Slew Rate for any signal		1.25	1

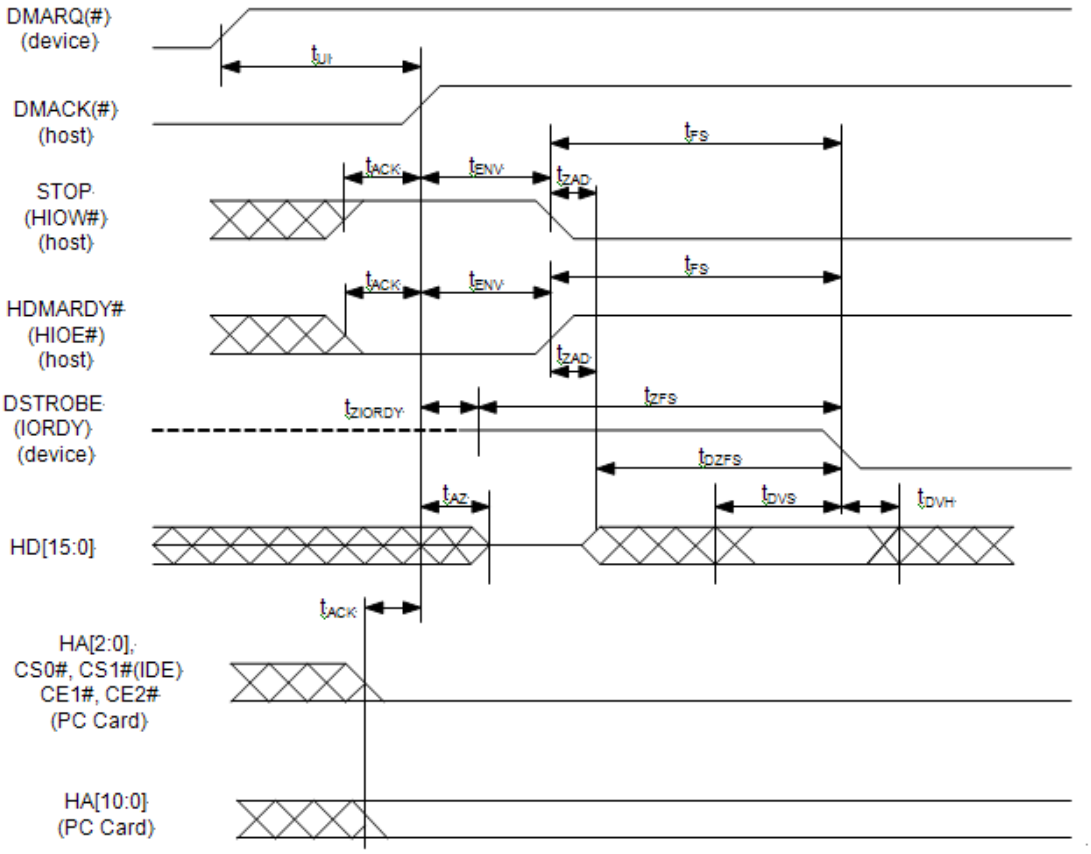
Note:

1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

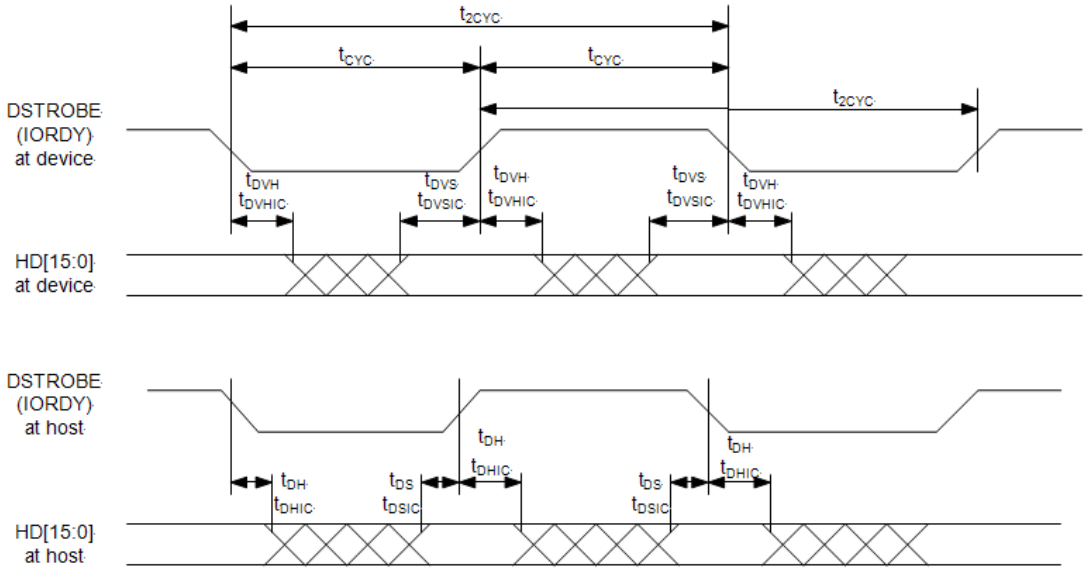
   The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

   Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

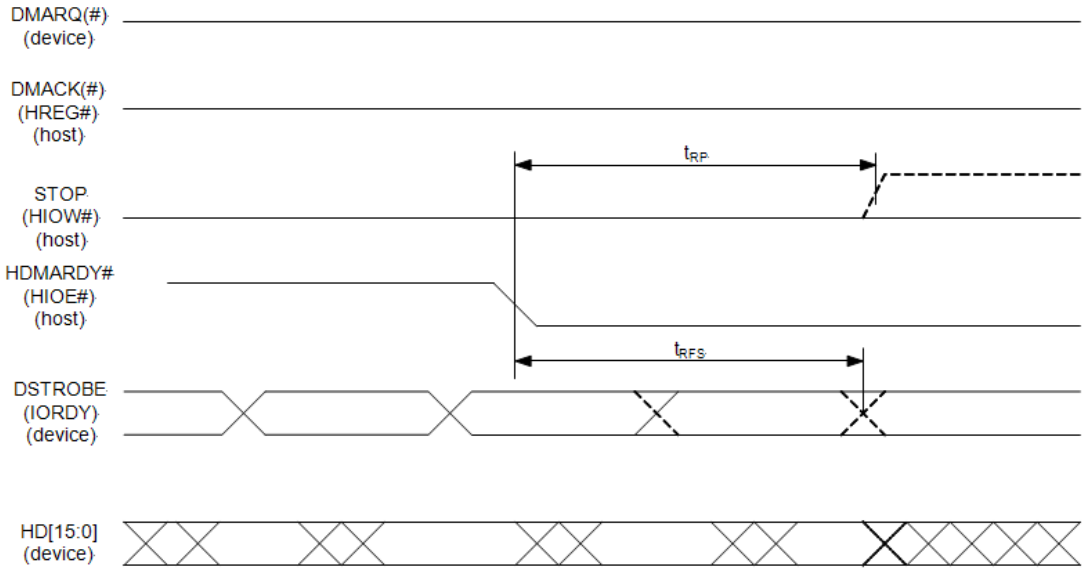
■ Ultra DMA Data-In Burst Initiation Timing



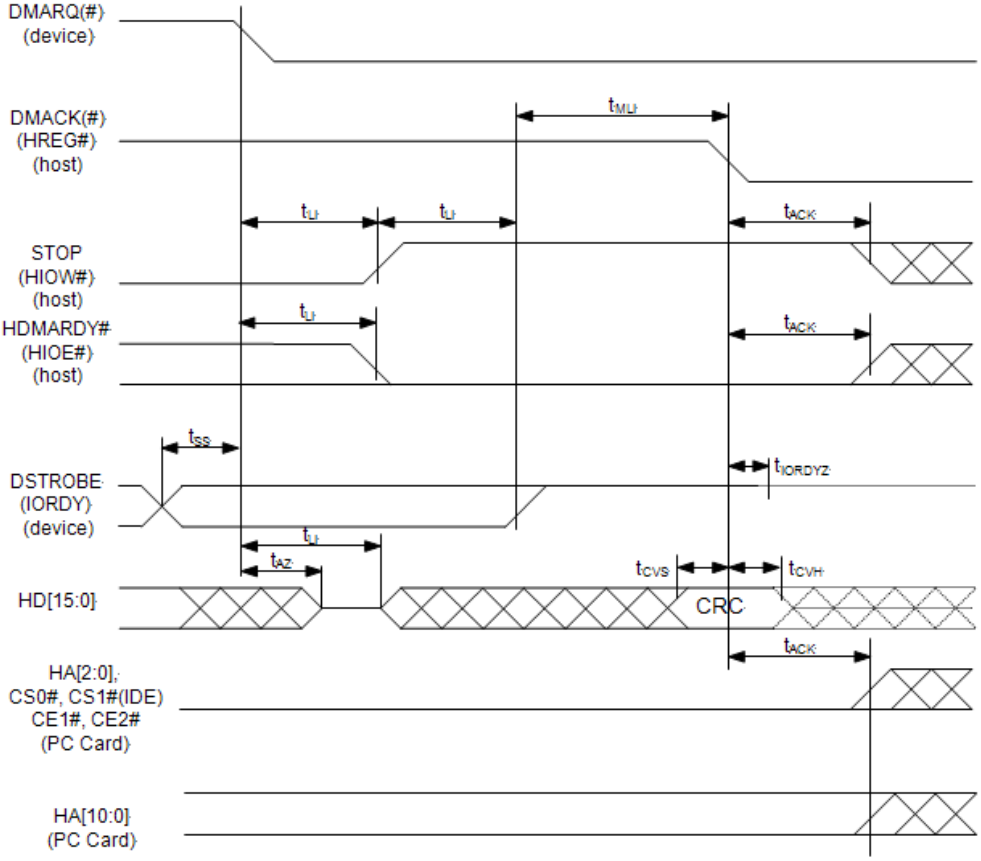
■ Sustained Ultra DMA Data-In Burst Timing



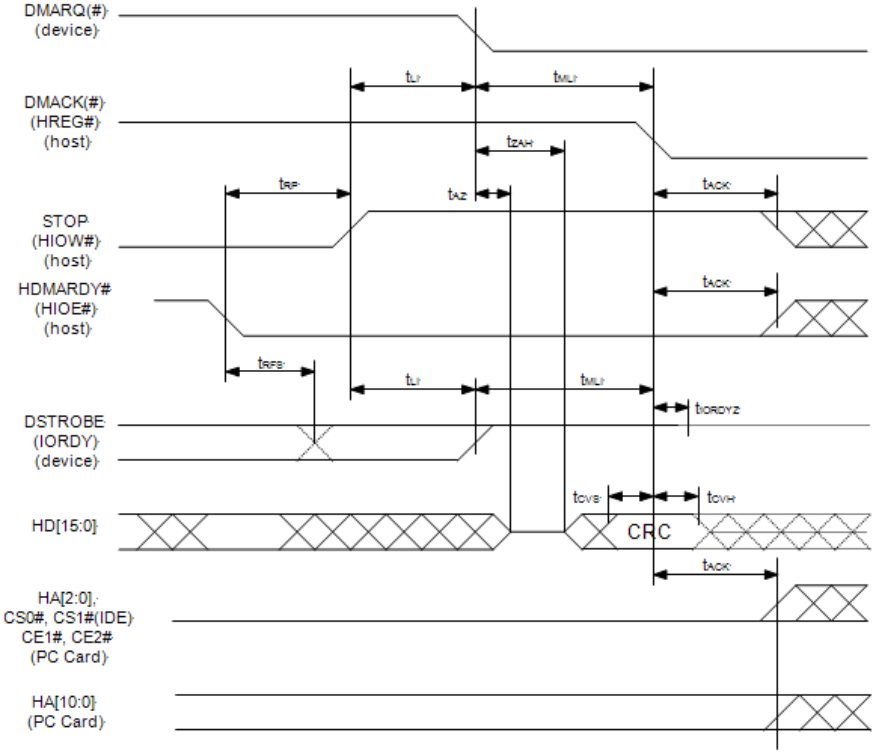
■ Ultra DMA Data-In Burst Host Pause Timing



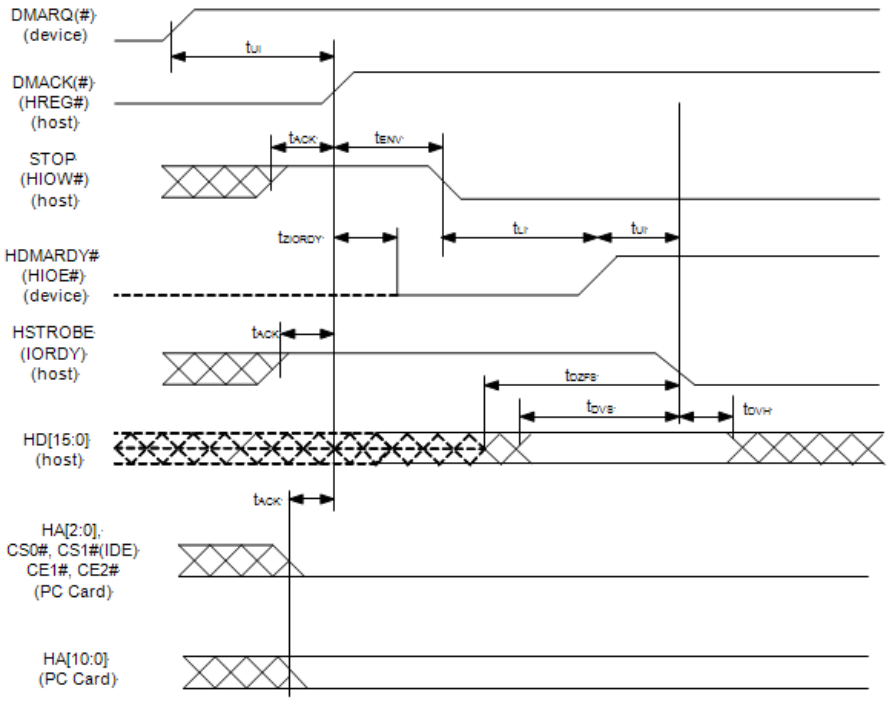
■ Ultra DMA Data-In Burst Device Termination Timing



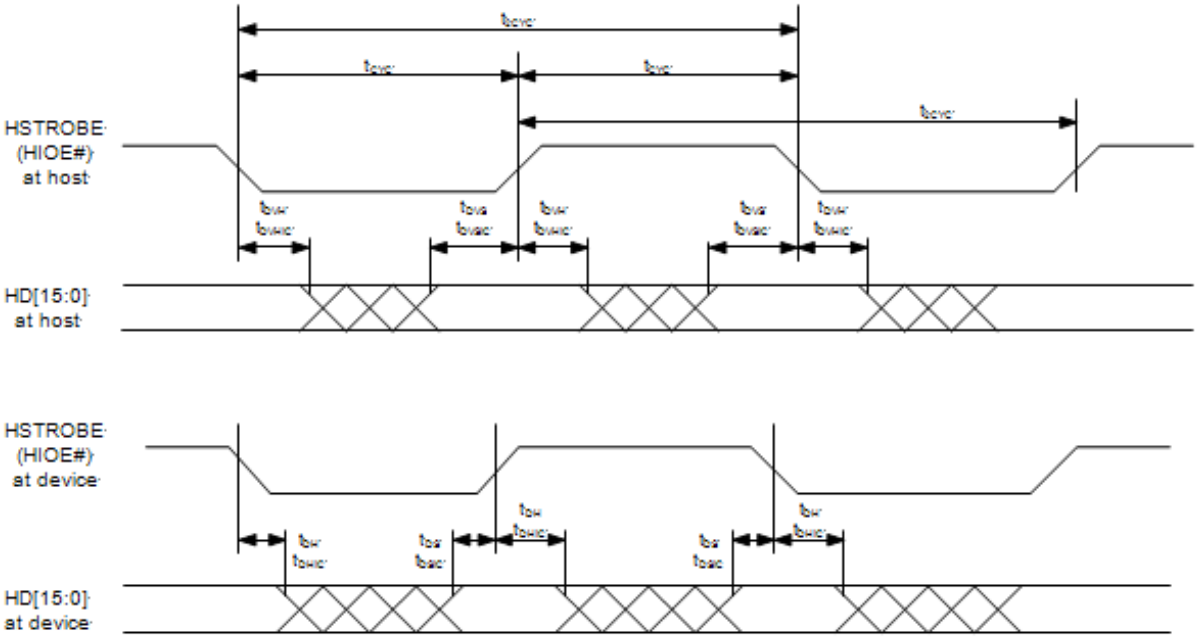
■ Ultra DMA Data-In Burst Host Termination Timing



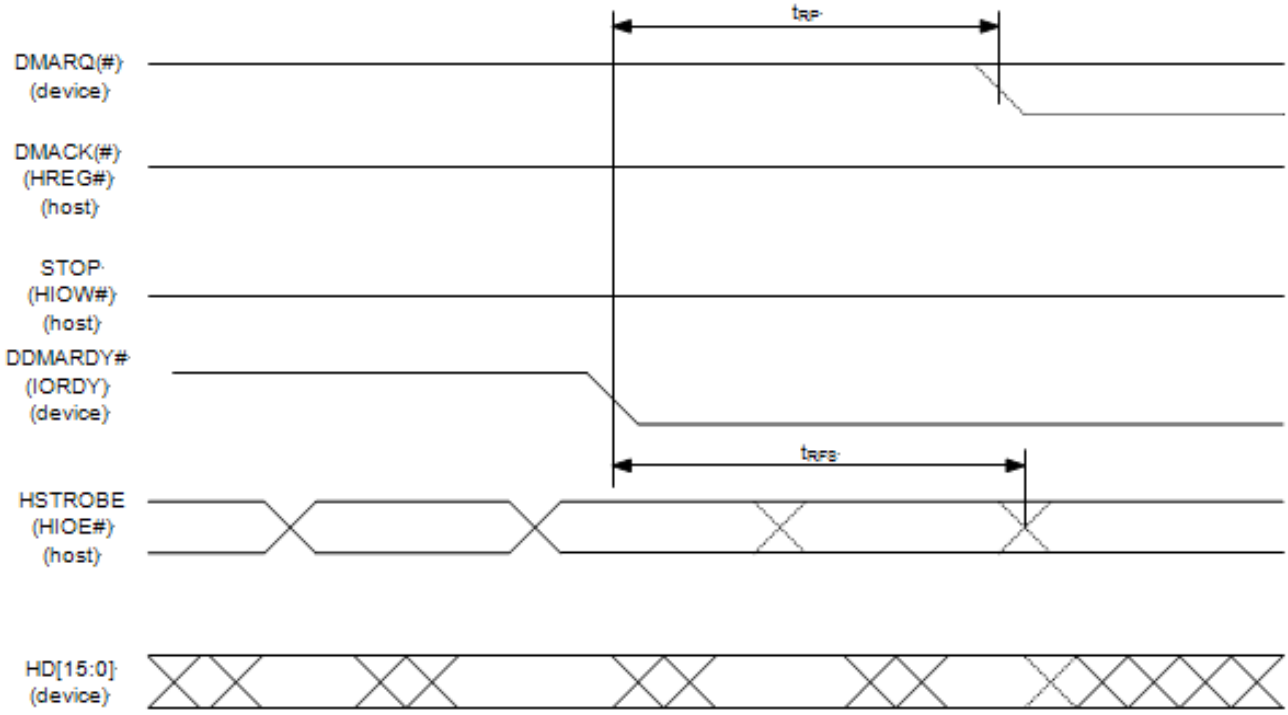
■ Ultra DMA Data-Out Burst Initiation Timing



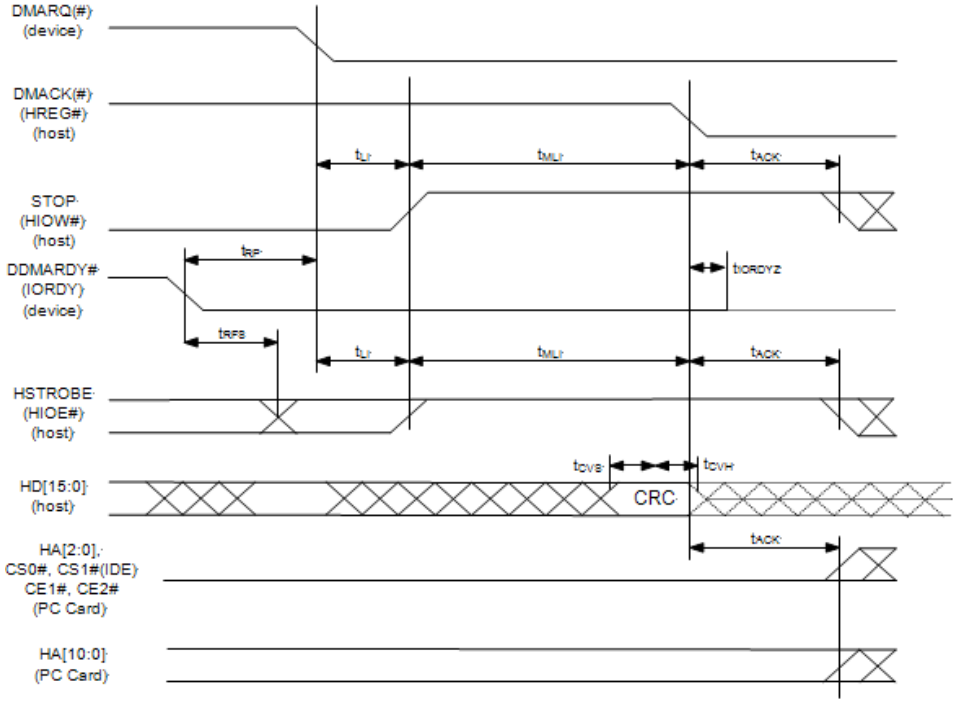
■ Sustained Ultra DMA Data-Out Burst Timing



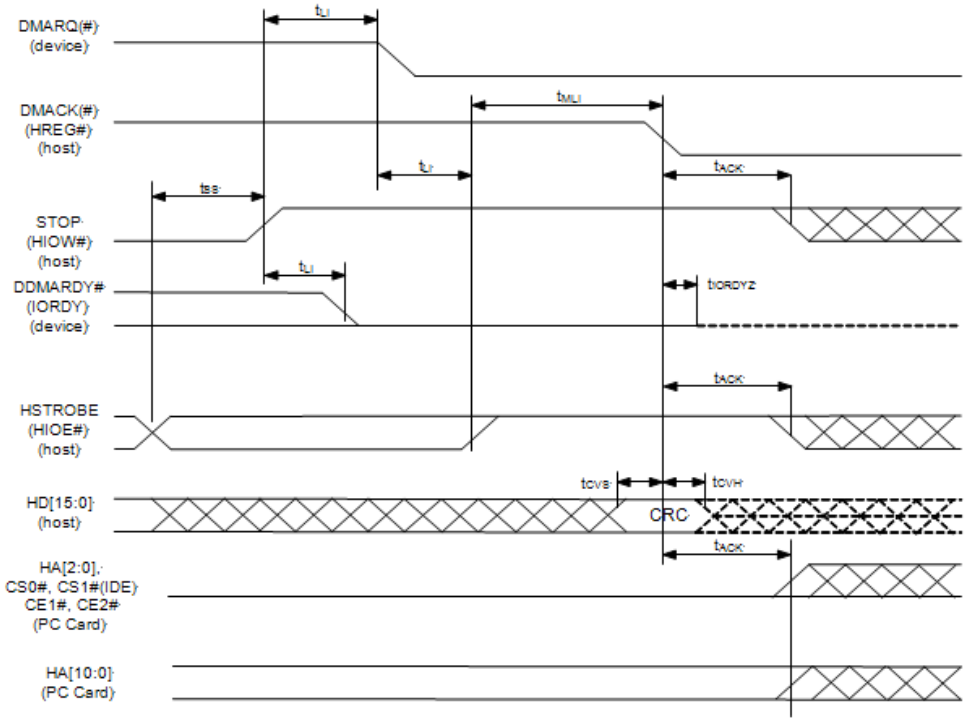
■ Ultra DMA Data-Out Burst Device Pause Timing



■ Ultra DMA Data-Out Burst Device Termination Timing



■ Ultra DMA Data-Out Burst Host Termination Timing



■ ATA/ATAPI Command List

Command	Code	Protocol
General Feature Set		
EXECUTE DIAGNOSTICS	90h	Device diagnostic
FLUSH CACHE	E7h	Non-data
IDENTIFY DEVICE	ECh	PIO data-In
READ DMA	C8h	DMA
READ MULTIPLE	C4h	PIO data-In
READ SECTOR(S)	20h or 21h	PIO data-In
READ VERIFY SECTOR(S)	40h or 41h	Non-data
SET FEATURES	EFh	Non-data
SET MULTIPLE MODE	C6h	Non-data
WRITE DMA	CAh	DMA
WRITE MULTIPLE	C5h	PIO data-out
WRITE SECTOR(S)	30h or 31h	PIO data-out
NOP	00h	Non-data
READ BUFFER	E4h	PIO data-In
WRITE BUFFER	E8h	PIO data-out
Power Management Feature Set		
CHECK POWER MODE	E5h or 98h	Non-data
IDLE	E3h or 97h	Non-data
IDLE IMMEDIATE	E1h or 95h	Non-data
SLEEP	E6h or 99h	Non-data
STANDBY	E2h or 96h	Non-data
STANDBY IMMEDIATE	E0h or 94h	Non-data
Security Feature Set		
SECURITY SET PASSWORD	F1h	PIO data-out
SECURITY UNLOCK	F2h	PIO data-out
SECURITY ERASE PREPARE	F3h	Non-data
SECURITY ERASE UNIT	F4h	PIO data-out
SECURITY FREEZE LOCK	F5h	Non-data
SECURITY DISABLE PASSWORD	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-In
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out

■ General Feature Set

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This command reads out 512 Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

Identify Device Information Default Value

Word Address	Default value (Hex)	Total Bytes	Data Field Type Information
0	0x044A	2	General configuration
1	0xXXXX	2	Default number of cylinders
2	0x0000	2	Reserved
3	0x00XX	2	Default number of heads
4-5	0x02400000	4	Obsolete
6	0xXXXX	2	Default number of sectors per track
7 - 8	0xXXXXXXXX	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0x0000	2	Obsolete
10 - 19	0xXXXX	20	Serial number in ASCII (Right justified)
20	0x0002	2	Obsolete
21	0x0002	2	Obsolete
22	0x0004	2	Obsolete
23 - 26	0xXXXX	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27 - 46	0xXXXX	40	Model number in ASCII (Left justified). Big Endian Byte Order in Word.
47	0x8001	2	Maximum number of sectors on Read/Write Multiple command
48	0x0000	2	Reserved
49	0x0F00	2	Capabilities
50	0x4000	2	Capabilities
51	0x0200	2	PIO data transfer cycle timing mode
52	0x0000	2	Obsolete
53	0x0007	2	Field validity
54	0xXXXX	2	Current numbers of cylinders
55	0xXXXX	2	Current numbers of heads
56	0xXXXX	2	Current sectors per track

Word Address	Default value (Hex)	Total Bytes	Data Field Type Information
57 - 58	0xXXXX	4	Current capacity in sectors (LBAs) (Word57 = LSW , Word58 = MSW)
59	0x0000	2	Multiple sector setting
60 - 61	0xXXXX	4	Total number of sectors addressable in LBA Mode
62	0x0000	2	Reserved
63	0x0007	2	Multiword DMA transfer
64	0x0003	2	Advanced PIO modes supported
65	0x0078	2	Minimum Multiword DMA transfer cycle time per word
66	0x0078	2	Recommended Multiword DMA transfer cycle time.
67	0x0078	2	Minimum PIO transfer cycle time without flow control
68	0x0078	2	Minimum PIO transfer cycle time with lORDY flow control
69 -79	0x0000	22	Reserved
80	0x0800	2	Major version number (ATAPI-8)
81	0x0000	2	Minor version number
82	0x7028	2	Command sets supported 0
83	0x5000	2	Command sets supported 1
84	0x4000	2	Command sets supported 2
85	0x0000	2	Command sets enabled 0
86	0x0000	2	Command sets enabled 1
87	0x0000	2	Command sets enabled 2
88	0x007F	2	Ultra DMA mode supported and selected
89	0x0000	2	Time required for Security erase unit completion
90	0x0000	2	Time required for Enhanced security erase unit completion
91	0x0000	2	Current Advanced power management value
92	0x0000	3	Master Password Revision Code
93	0x604F 0x6F00 0x603F	2	• Hardware reset result (Master only) • Hardware reset result (Slave only) • Hardware reset result (Master w/ slave present)
94 - 127	0x0000	68	Reserved
128	0x0001	2	Security Status
129-159	0xXXXX	62	Vendor specific
160	0x0000	2	Power requirement description
161	0x0000	2	Reserved
162	0x0000	2	Key management schemes support
163	0x0000	2	CF Advanced True IDE Timing Mode Capability and Setting
164	0x0000	2	• CF Advanced PCMCIA I/O and Memory Timing Mode Capability and Setting • 80 ns cycle in memory and I/O mode
165 - 175	0x0000	22	Reserved
176 - 255	0x0000	160	Reserved

READ DMA (C8h)

Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h or 21h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

SET FEATURES (EFh)

This command sets parameter to Features register and sets drive's operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE MULTIPLE (C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE SECTOR(S) (30h or 31h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify "00h" to write 256 sectors.

NOP (00h)

The device shall respond with command aborted. For devices implementing the Overlapped feature set, subcommand code 00h in the Features register shall abort any outstanding queue. Subcommand codes 01h through FFh in the

Features register shall not affect the status of any outstanding queue.

READ BUFFER (E4h)

The READ BUFFER command enables the host to read a 512-byte block of data.

WRITE BUFFER (E8h)

This command enables the host to write the contents of one 512-byte block of data to the device's buffer.

■ Power Management Feature Set

CHECK POWER MODE (E5h or 98h)

The host can use this command to determine the current power management mode.

IDLE (E3h or 97h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h or 95h)

This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

SLEEP (E6h or 99h)

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

STANDBY (E2h or 96h)

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h or 94h)

This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

■ Security Mode Feature Set

SECURITY SET PASSWORD (F1h)

This command sets user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

Security set Password data content1

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set user password 1=set master password
	Bits 1-7	Reserved	
	Bit 8	Security level	0=High 1=Maximum
	Bits 9-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY UNLOCK (F2h)

This command disables LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

Security Unlock information2

Word	Content		
0	Control word		
	Bit 0	Identifier	0=compare user password 1=compare master password
	Bits 1-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

■ SMART Feature Set

Transcend's IDE SSD supports the SMART command set and defines some vendor-specific data to report spare/bad block numbers in each memory management unit. Individual SMART commands are identified by the value placed in the Feature register. The table below shows these Feature register values.

SMART Feature Register Values			
D0h	Read Data	D5h	Reserved
D1h	Read Attribute Threshold	D6h	Reserved
D2h	Enable/Disable Autosave	D8h	Enable SMART Operations
D3h	Save Attribute Values	D9h	Disable SMART Operations
D4h	Execute OFF-LINE Immediate	DAh	Return Status

SMART DISABLE OPERATIONS

B0h with a Feature register value of D9h.Disables the SMART function. Upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then back on.

Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the Aborted Command error.

This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data in no longer be monitored or saved. The state of SMART is preserved across power cycles.

SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE

B0h with a Feature register value of D2h.Enables or disables the attribute value autosave function. This command specifies whether the current attribute values are automatically saved to the drive when it changes the mode. This setting is maintained when the power is turned on and off.

SMART ENABL OPERATIONS

B0h with a Feature register value of D8h.Enables the SMART function. This setting is maintained when the power is turned off and then back on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameters

SMART EXECUTE OFF-LINE IMMEDIATE

B0h with the content of the Features register equals to D4h. This command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory, or execute a self-diagnostic test routine in either captive or off-line mode.

SMART RETURN STATUS

B0h with a Feature register value of DAh. This command causes the device to communicate the reliability status of the device to the host. If a threshold exceeded condition is not detected by the device, the device shall set the LBA Mid register to 4Fh and the LBA High register to C2h. If a threshold exceeded condition is detected by the device, the device shall set the LBA Mid register to F4h and the LBA High register to 2Ch.

SMART Read Data

B0h with the content of the Features register equals to D0h. This command returns the Device SMART data structure to the host.

SMART DATA Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data by SMART command.

BYTE	F / V	Description
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396-399	R	Reserved
400-406	F	'SMI2236'
407-511	R	Reserved

F=the content of the byte is fixed and does not change.

V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.

X=the content of the byte is vendor specific and may be fixed or variable.

R=the content of the byte is reserved and shall be zero.

* 4 Byte value : [MSB] [2] [1] [LSB]

SMART Attributes

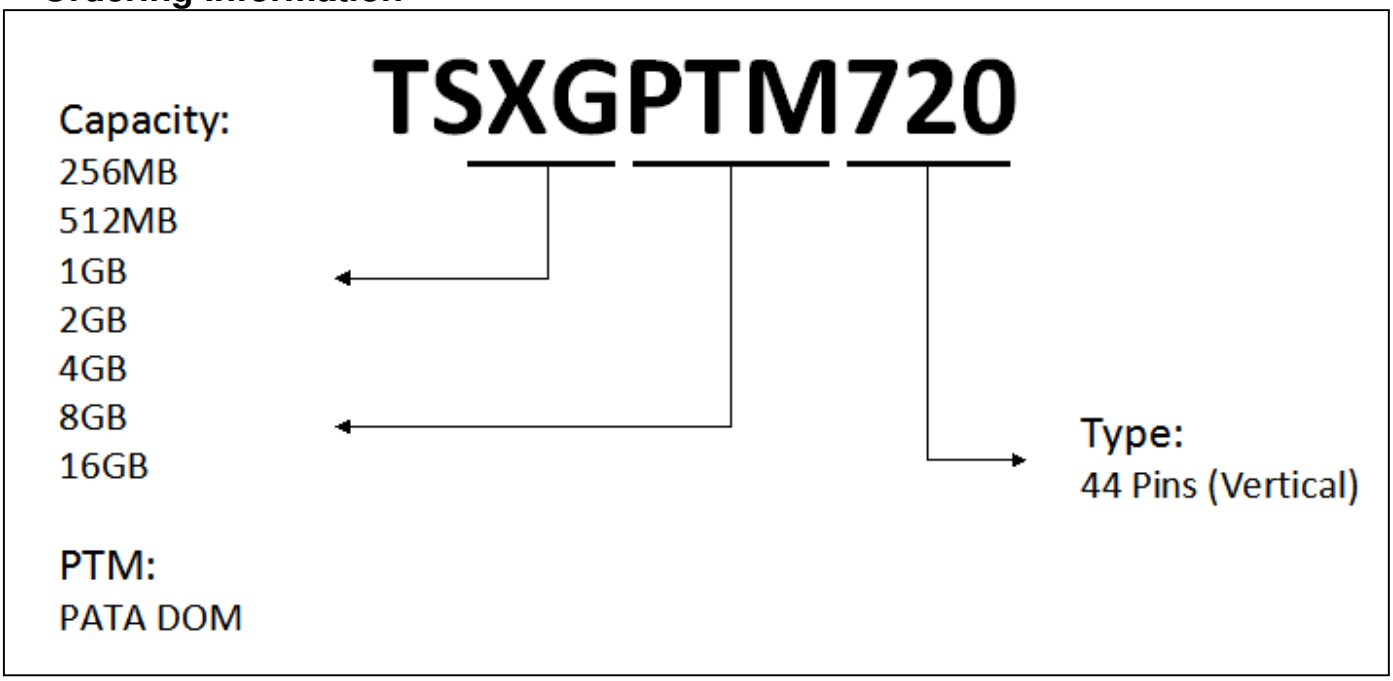
The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data.

Attribute ID(hex)	Raw Attribute Value						Attribute Name
01	MSB	00	00	00	00	00	Read Error Rate
05	LSB	MSB	00	00	00	00	Reallocated Sectors Count
0C	LSB	MSB	00	00	00	00	Power Cycle Count
A1	LSB	MSB	00	00	00	00	Number of Valid Spare Block
A2	LSB	MSB	00	00	00	00	Number of child pair
A3	LSB	MSB	00	00	00	00	Number of initial invalid Block
A4	LSB	~	~	MSB	00	00	Total erase count
A5	LSB	~	~	MSB	00	00	Maximum Erase Count
A6	LSB	~	~	MSB	00	00	Minimum Erase Count
A7	LSB	~	~	MSB	00	00	Average Erase Count
C0	LSB	MSB	00	00	00	00	Power-Off Retract Count
C7	LSB	MSB	00	00	00	00	Ultra DMA CRC Error Rate

■ Host Protected Area Feature Set

A reserved area for data storage outside the normal operating system file system is required for several specialized applications. Systems may wish to store configuration data or save memory to the device in a location that the operating systems cannot change. The optional Host Protected Area feature set allows a portion of the device to be reserved for such an area when the device is initially configured.

■ Ordering Information



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Revision History

Version	Date	Modification Content	Modified Page
V1.0	2015/04/01	Initial beta release	