RoHS Compliant

Industrial Secure Digital Card

Product Specifications

April 21, 2016

Version 1.1

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FEATURES:

- **Fully Compatible with SD Card Standard Specification**
  - SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 2.00
  - SD Memory Card Specifications, Part 2, File System Specification, Version 2.00
  - SD Memory Card Specifications, Part 3, Security Specification, Version 2.00
- **Capacity**
  - Standard: 256, 512 MB
    1, 2 GB
  - SDHC: 4, 8, 16, 32 GB
- **Performance**
  - Sustained read: Up to 23 MB/sec
  - Sustained write: Up to 17 MB/sec
- **SD-Protocol Compatible**
- **Support SPI Mode**
- **NAND Flash Type:** SLC
- **Endurance (TBW: Terabytes Written)**
  - 256MB: 3 TBW
  - 512MB: 6 TBW
  - 1 GB: 12 TBW
  - 2 GB: 24 TBW
  - 4 GB: 49 TBW
  - 8 GB: 98 TBW
  - 16 GB: 196 TBW
- **Variable Clock Rate 0-50MHz**
- **Flash Management**
  - Built-in BCH-ECC supports correction up to 24 bits data error per 1K bytes data automatically
  - Implements wear-leveling algorithms to substantially increase longevity of flash media
  - Flash bad-block management
  - S.M.A.R.T utility
- **Temperature Range**
  - Operating temperature
    Standard: 0°C to 70°C
    Extended: -40°C to 85°C
  - Storage temperature: -40°C ~ 85°C
- **Power Consumption**
  - Standby: 110 µA
  - Read: 45 mA
  - Write: 55 mA
- **Operation Voltage:** 2.7V ~ 3.6V
- **Physical Dimensions:** 24 x 32 x 2.1
  (unit : mm)
- **RoHS Compliant**

Note: The performance and the power consumption addressed here are typical and may vary from capacities, flash configurations or host system settings.

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Table of Contents

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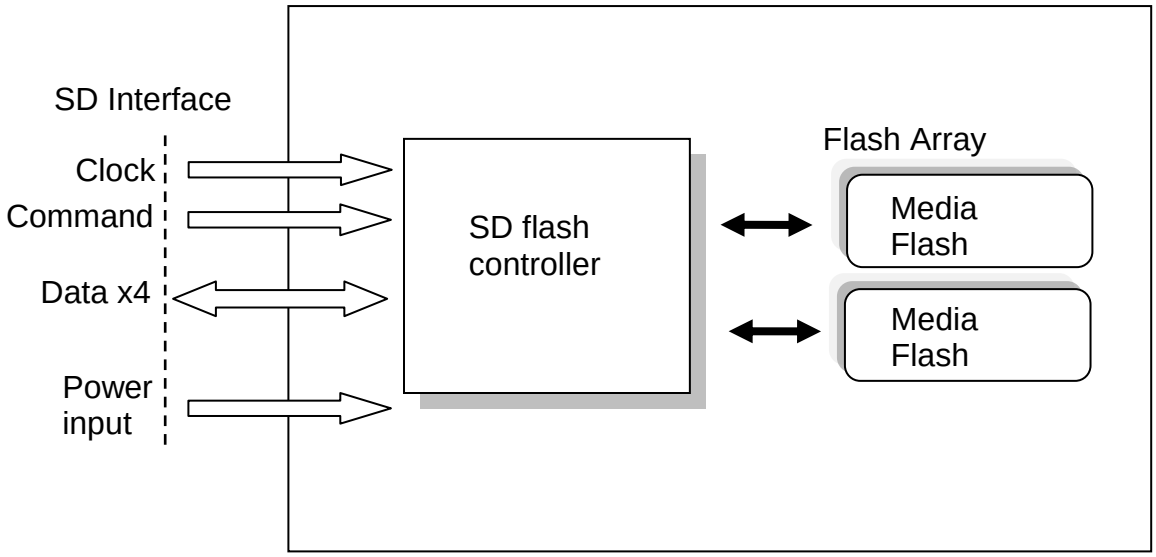
1. General Description

As the demand of reliable and high-performance data storage in a small form factor increases, Apacer's embedded SD card is designed specifically for rigorous applications by offering maximum endurance, reliability, and agility, where extreme traceability, enhanced data integrity, and exceptionally velocity are required.

1.1 Product Function Block

The embedded SD contains a flash controller and flash media with SD standard interface.



1.2 Functional Description

The embedded SD device contains a high level, intelligent subsystem that provides many capabilities including:

- Powerful ECC algorithms
- Wear-leveling algorithms
- Power management

1.2.1 Flash Management

The SD controller contains logic/physical flash block mapping and bad block management system. It will manage all flash block include user data space and spare block.

The embedded SD also contains a sophisticated defect and error management system. It does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the embedded SD replaces this bad bit with a spare bit within the sector header. If necessary, the embedded SD will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

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1.2.2 Powerful ECC Algorithms

The powerful ECC algorithms will enhance flash block use rate and whole device life. The SD controller has an innovative algorithm to recover the data. Built-in BCH-ECC supports correction up to 24 bits data error per 1K bytes data automatically

1.2.3 Power Management

A power saving feature of the embedded SD is automatic entrance and exit from sleep mode. Upon completion of an operation, the embedded SD will enter the sleep mode to conserve power if no further commands are received within X seconds, where X is programmable by software. The master does not have to take any action for this to occur. The embedded SD is in sleep mode except when the host is accessing it, thus conserving power.

Any command issued by the master to the embedded SD will cause it to exit sleep mode and response to the master.

1.2.4 S.M.A.R.T

S.M.A.R.T. (SMART), an acronym stands for Self-Monitoring, Analysis and Reporting Technology, is an open standard allowing an individual disk drive in the ATA/IDE or SCSI interface to automatically monitor its own health and report potential problems in order to prevent data loss. This failure warning technology provides predictions from unscheduled downtime by observing and storing critical drive performance and calibration parameters. Ideally, this should allow taking hands-on actions to keep from impending drive failure.

Failures are divided into two categories: those that can be predicted and those that cannot. Predictable failures occur gradually over time, and the decline in performance can be detected; on the other hand, unpredictable failures happen very sudden without any warning. These failures may be caused by power surges or related to electronic components. The purpose of the SMART implementation is to predict near-term failures of each individual disk drive and generate a warning to prevent unfortunate loss.

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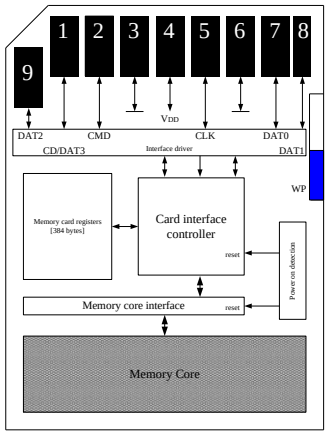
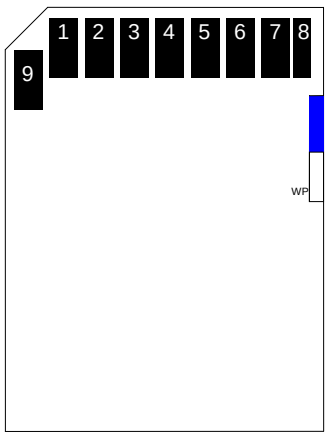
2. Electrical characteristics

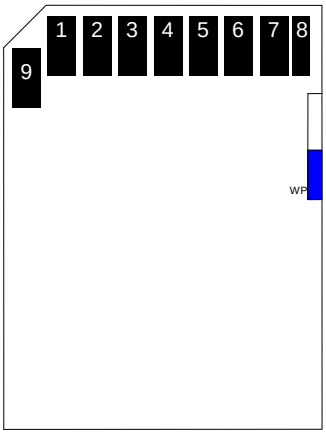
2.1 Card Architecture



Write Enabled



Write Protected



2.2 Pin Assignment

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	CD/DAT3	Card detect/Data line[Bit 3]	CS	Chip select
2	CMD	Command/Response	DI	Data in
3	VSS1	Supply voltage ground	VSS	Supply voltage ground
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS2	Supply voltage ground	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]	DO	Data out
8	DAT1	Data line[Bit 1]	Reserved	
9	DAT2	Data line[Bit 2]	Reserved	

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2.3 Capacity Specifications

The following table shows the out-of-box capacity. (Follow SDA rule to do format)

Capacity	Total (LBA) Sectors	Total Partition Sectors	User Data Sectors	User Data Bytes
256 MB	499,712	499,611	499,456	255,721,472
512 MB	985,088	984,851	984,576	504,102,912
1 GB	2,000,896	2,000,651	2,000,128	1,024,065,536
2 GB	4,009,984	4,009,739	4,009,216	2,052,718,592
4 GB	8,019,968	8,011,776	8,003,584	4,097,835,008
8 GB	16,039,936	16,031,744	16,023,552	8,204,025,856
16 GB	31,719,424	31,711,232	31,703,040	16,231,923,712
32 GB	63,438,848	63,430,656	63,414,272	32,468,074,496

Note: The statistics may vary depending on file systems of various OS. User data bytes do not indicate total useable bytes. LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

2.4 Performance

Performances of Embedded SD are shown in the table below.

Capacity / Performance	256 MB	512 MB	1 GB	2 GB	4 GB	8 GB	16 GB	32 GB
Sustained Read (MB/s)	22	23	23	23	23	23	23	23
Sustained Write (MB/s)	11	17	17	18	17	17	16	17

Note: Performances vary from flash configurations or host device settings.

2.5 Endurance

The endurance of a storage device is predicted by Tera Bytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Capacity	Tera Bytes Written
256MB	3
512MB	6
1 GB	12
2 GB	24
4 GB	49
8 GB	98
16 GB	196

Note:

- The measurement assumes the data written to the SSD for test is under a typical and constant rate.
- The measurement follows the standard metric: 1 TB (Terabyte) = 1,000 GB.
- The estimated values are based on JEDEC Enterprise endurance workload comprised of random data with the payload size distribution with sequential write behavior.

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2.6 DC Power Supply

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	2.7	3.3	3.6	V

2.7 Power consumption

Mode	Value	Unit	Condition
Standby	110	µA	Typical
Read	45	mA	Typical
Write	55	mA	Typical

Note: Results are measured under 3.3V

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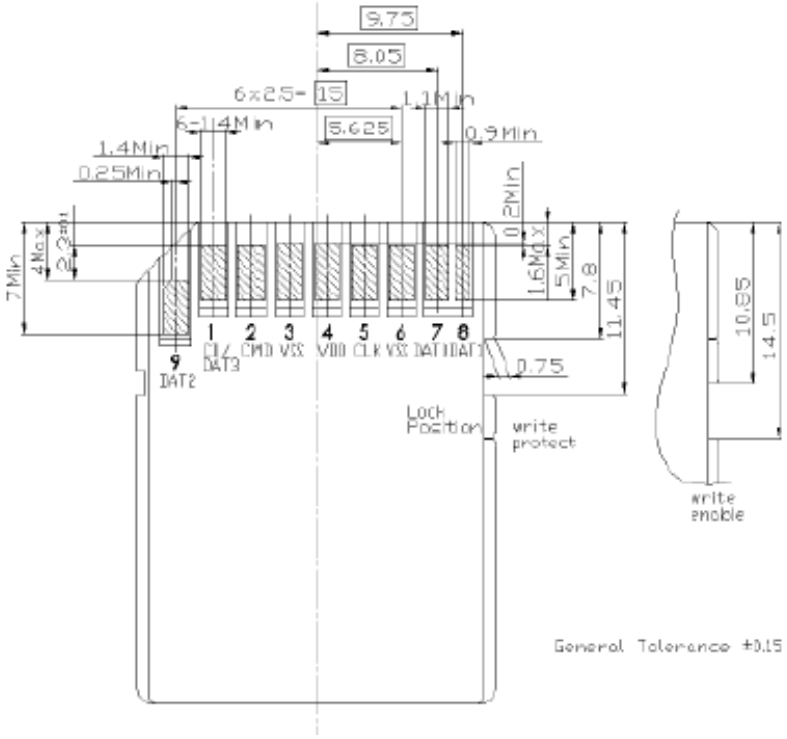
3. Physical Characteristics

3.1 Physical Dimensions

Dimensions Card Package	24 mm x 32 mm Min. 23.9 mm x 31.9 mm Max. 24.1 mm x 32.1 mm
Thickness	2.1 mm ± 0.15 mm
Surface	Plain (except contact area)
Edges	Smooth edges



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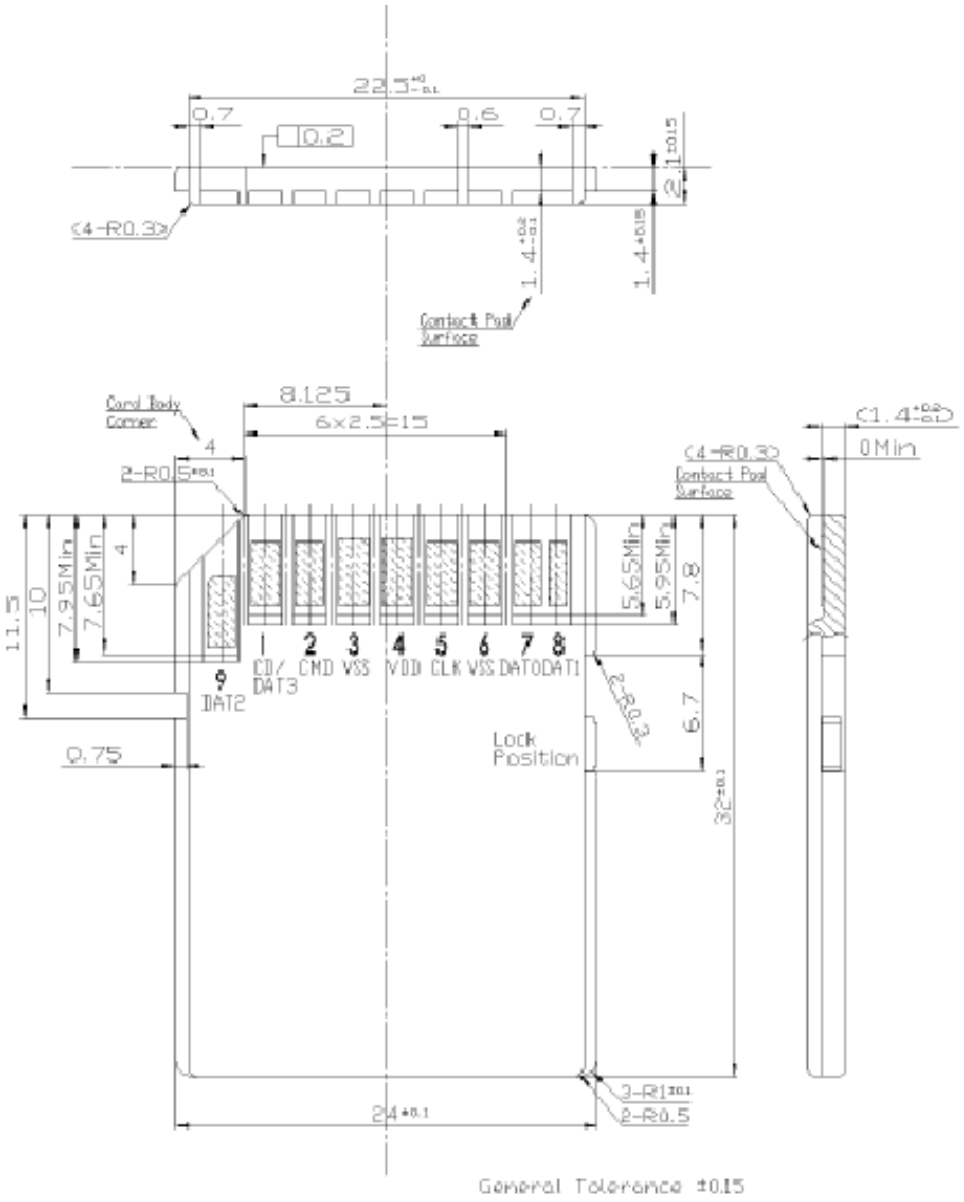

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3.2 Durability Specifications

Item	Specifications
Temperature	0°C to 70°C (Standard) -40°C to 85°C (Extended)
	-40°C to 85°C (Storage)
Shock	1,000G, 0.5ms
Vibration	10Hz~50Hz/3mm (frequency/displacement) 50Hz~2,000Hz/15G (frequency/accelerate) X, Y, Z axis/2 hours each
Drop	1.5m free fall, 10 times of each
Bending	≧10N, hold 1min/1 time
Torque	0.15N-m or 2.5deg, hold 30 seconds/1 time
Salt spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Switch cycle	0.4~5N, 1,000 times
Durability	10,000 times mating cycle

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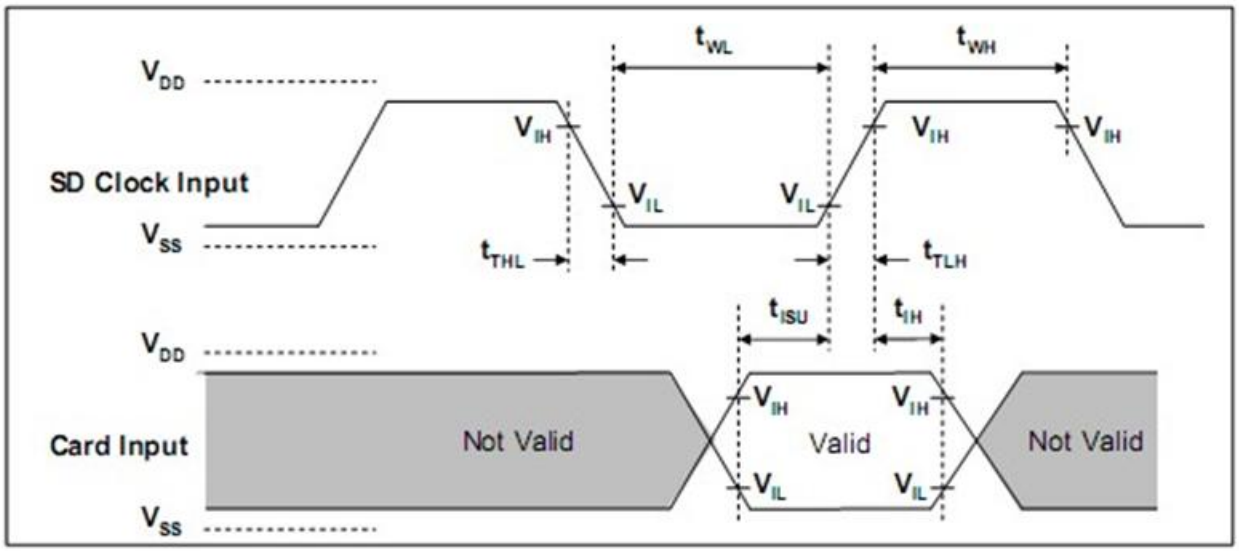
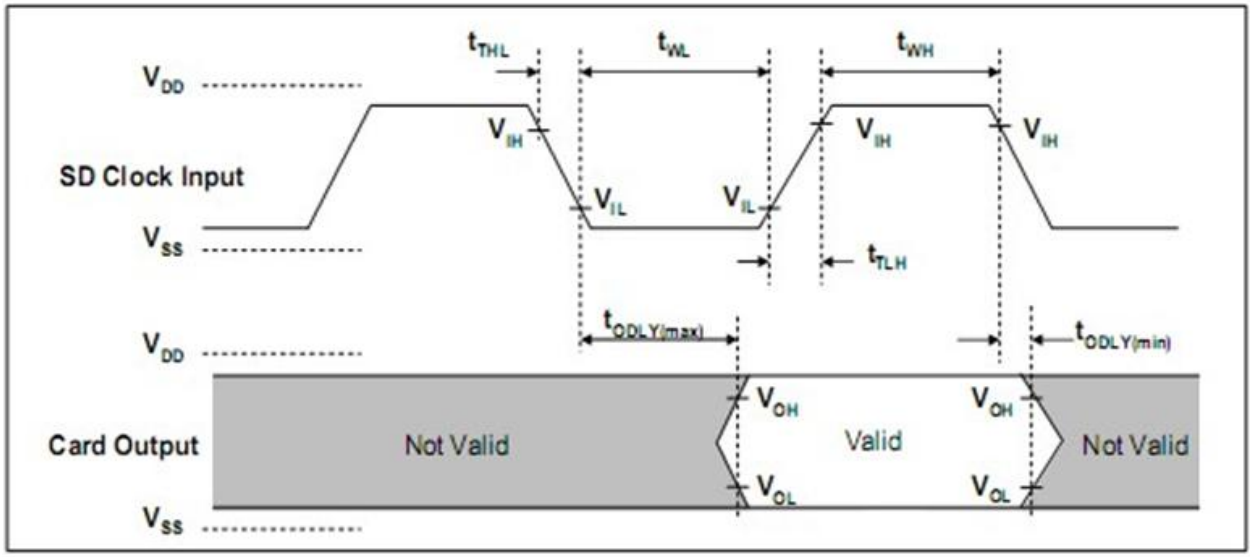
4. AC Characteristics

4.1 SD Interface Timing (Default)



Card input Timing (Default Speed Card)



Card Output Timing (Default Speed Mode)

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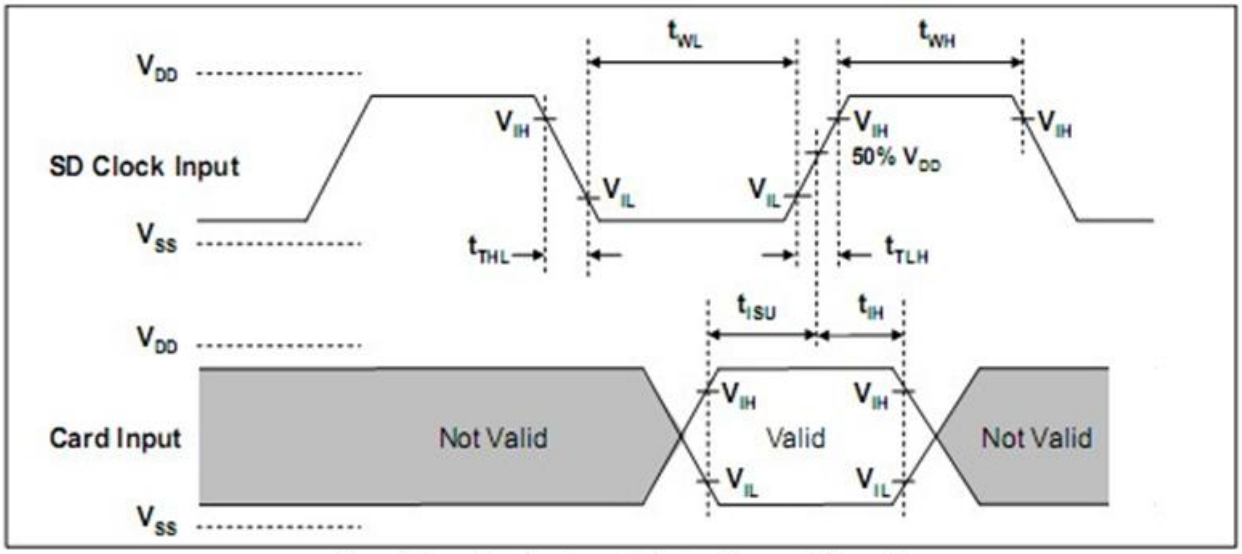
SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	25	MHz	C_{card} ≤ 10 pF (1 card)
f_{OD}	Clock frequency identification	0[(1)]/100	400	KHz	C_{card} ≤ 10 pF (1 card)
t_{WL}	Clock low time	10	-	ns	C_{card} ≤ 10 pF (1 card)
t_{WH}	Clock high time	10	-	ns	C_{card} ≤ 10 pF (1 card)
t_{TLH}	Clock rise time	-	10	ns	C_{card} ≤ 10 pF (1 card)
t_{THL}	Clock fall time	-	10	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	5	-	ns	C_{card} ≤ 10 pF (1 card)
t_{TH}	Input hold time	5	-	ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer mode	0	14	ns	C_L ≤ 40 pF (1 card)
t_{OH}	Output hold time	0	50	ns	C_L ≤ 40 pF (1 card)

(1)0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

4.2 SD Interface Timing (High Speed Mode)



Card Input Timing (High Speed Card)

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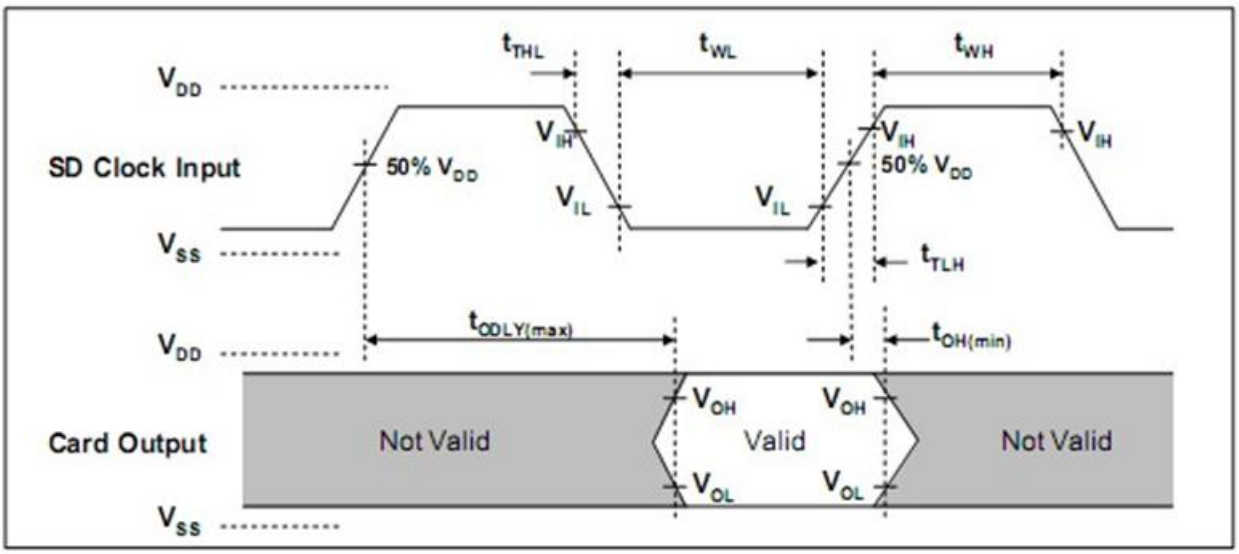

Card Output Timing (High Speed Mode)

SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	50	MHz	Ccard ≤ 10 pF (1 card)
t_{WL}	Clock low time	7	-	ns	Ccard ≤ 10 pF (1 card)
t_{WH}	Clock high time	7	-	ns	Ccard ≤ 10 pF (1 card)
t_{TLH}	Clock rise time	-	3	ns	Ccard ≤ 10 pF (1 card)
t_{THL}	Clock fall time	-	3	ns	Ccard ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	6	-	ns	Ccard ≤ 10 pF (1 card)
t_{TH}	Input hold time	2	-	ns	Ccard ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer made	-	14	ns	CL ≤ 40 pF (1 card)
t_{OH}	Output hold time	2.5	-	ns	CL ≥ 15 pF (1 card)
C_L	Total system capacitance for each line*	-	40	pF	1 card

***In order to satisfy severe timing, host shall run on only one card**

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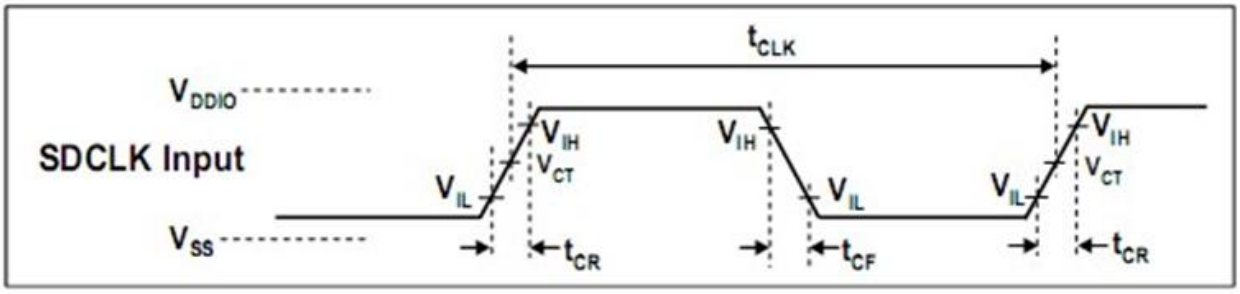
4.3 SD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes) Input

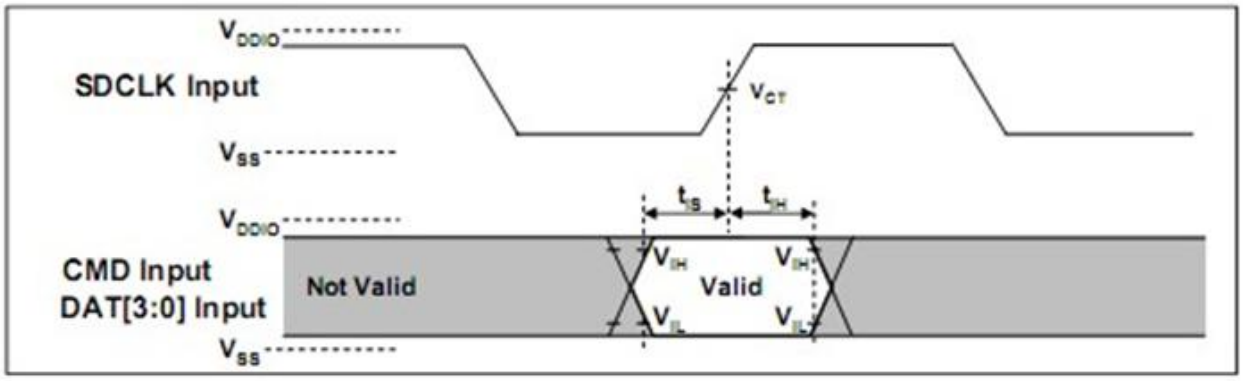
4.3.1 Clock Timing



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 2.00ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

4.3.2 Card Input Timing



Card Input Timing

SYMBOL	MIN	MAX	UNIT	SDR104 MODE
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
SYMBOL	**MIN**	**MAX**	**UNIT**	**SDR12, SDR25 and SDR50 MODES**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

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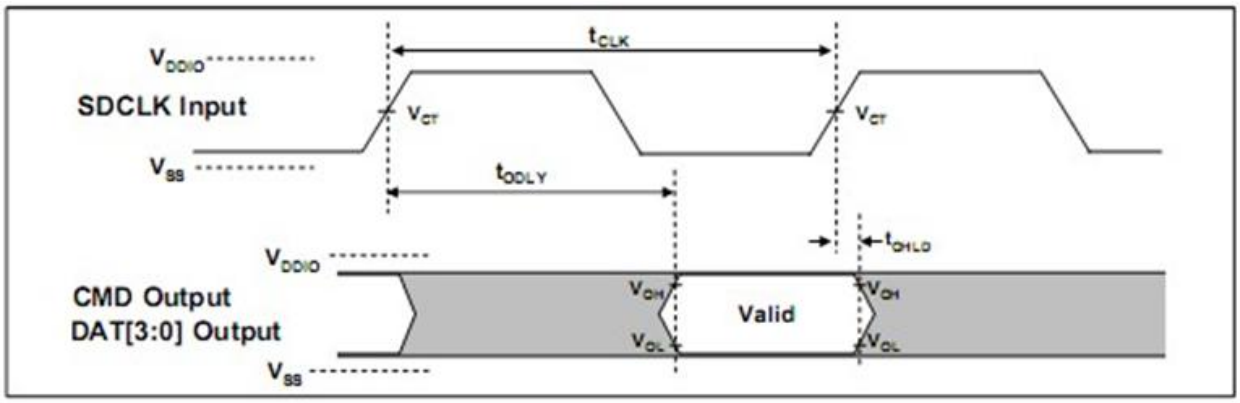
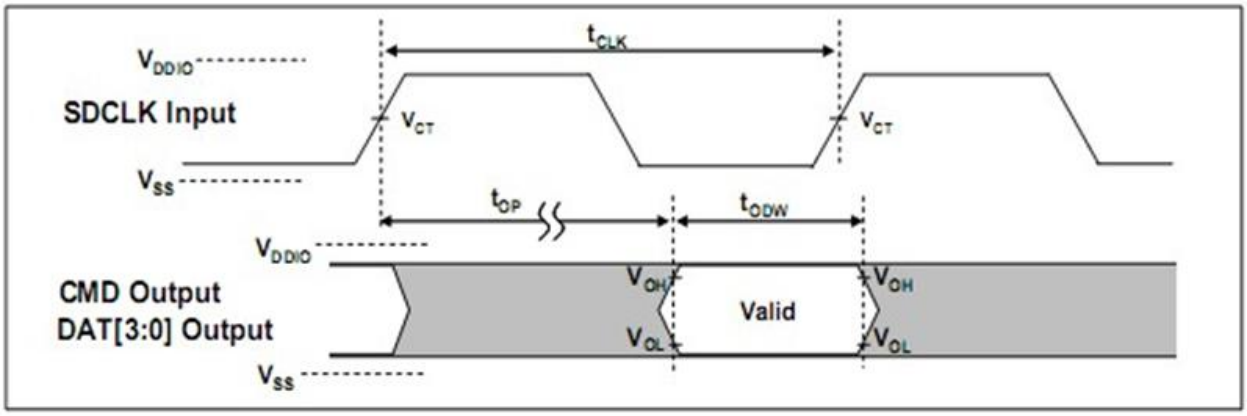
4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)



Output Timing of Fixed Date Window

SYMBOL	MIN	MAX	UNIT	REMARK
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, CL=30pF, using driver Type B, for SDR50.
t_{ODLY}		14	ns	t_{CLK} ≥20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12.
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). CL=15pF

4.3.4 Output Timing of Variable Window (SDR104)



Output Timing of Variable Data Window

SYMBOL	MIN	MAX	UNIT	REMARK
t_{OP}	-	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

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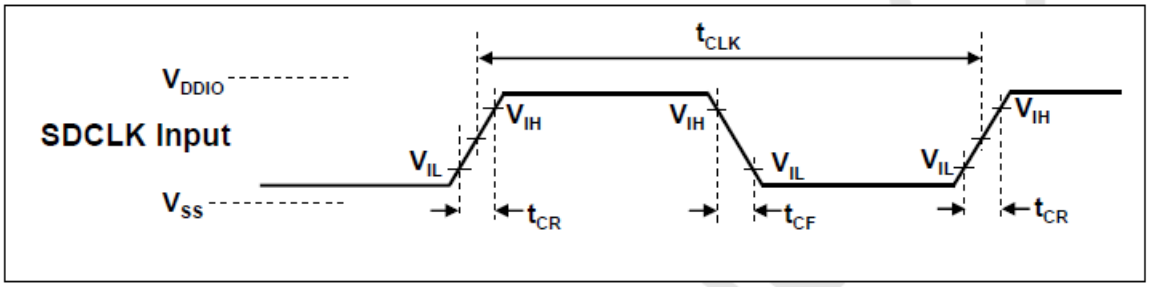
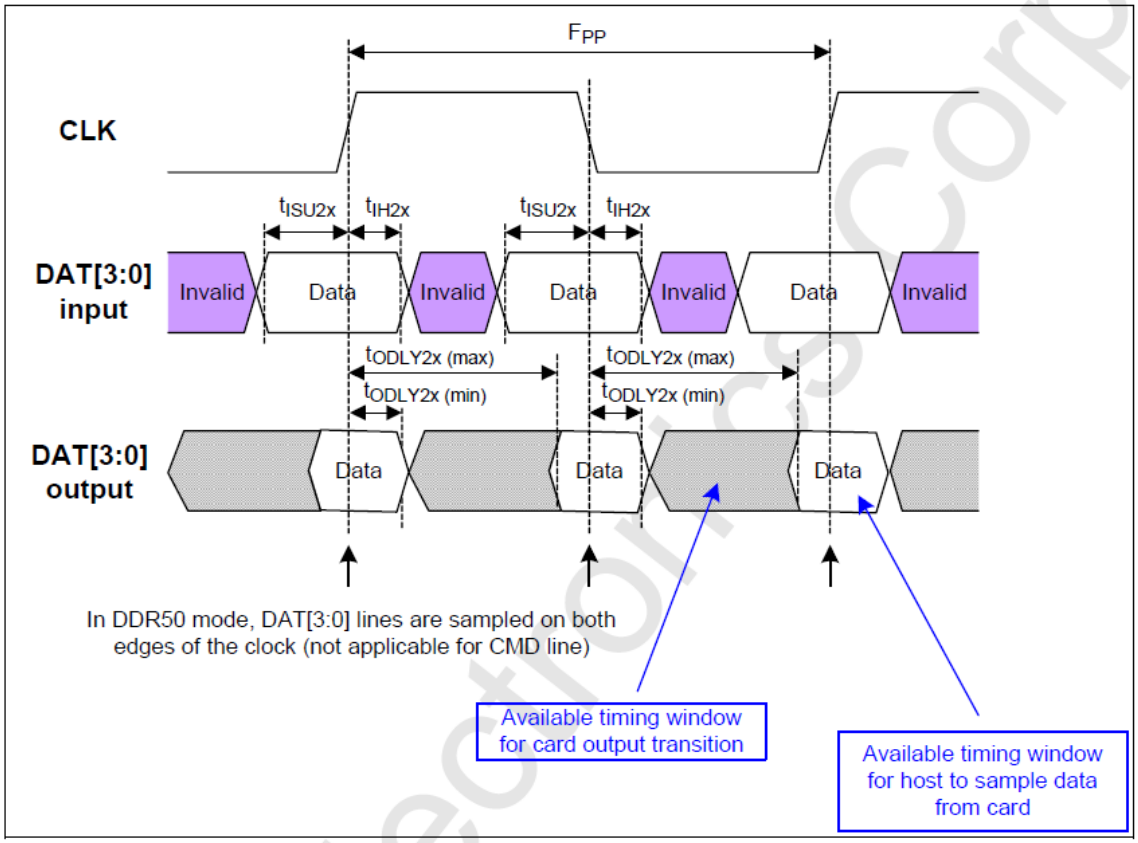
4.3.5 SD Interface Timing (DDR50 Mode)



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

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4.3.6 Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameters	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t_{ISU}	Input set-up time	6	-	ns	C_{card}≤ 10 pF (1 card)
t_{IH}	Input hold time	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
t_{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	C_L≤30 pF (1 card)
T_{OH}	Output Hold time	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t_{ISU2x}	Input set-up time	3	-	ns	C_{card}≤ 10 pF (1 card)
t_{IH2x}	Input hold time	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t_{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	C_L≤25 pF (1 card)
T_{OH2x}	Output Hold time	1.5	-	ns	C_L≥15 pF (1 card)

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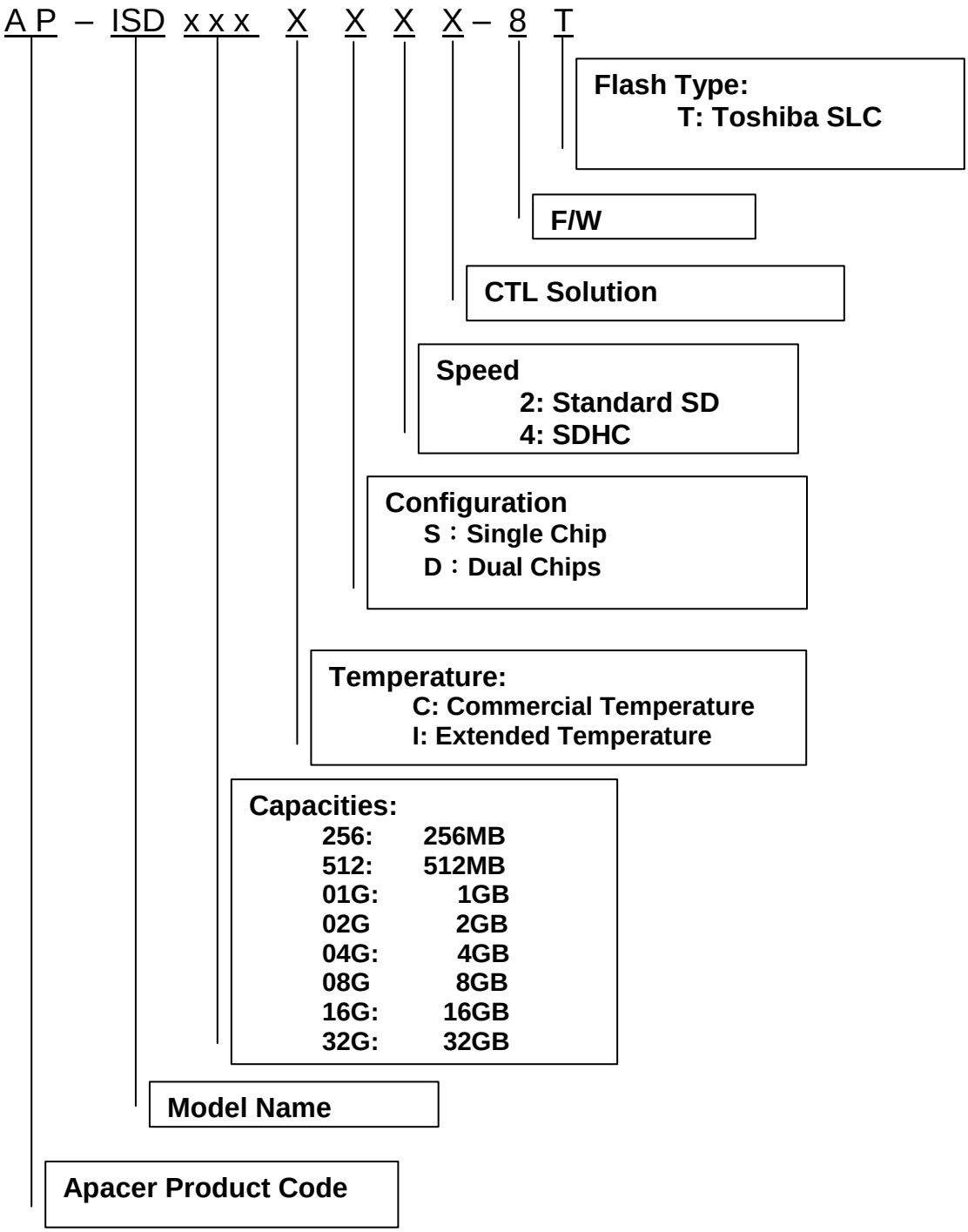
5. Product Ordering Information

5.1 Product Code Designations



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5.2 Valid Combinations

5.2.1 Standard Temperature

Capacity	AP/N
256 MB	AP-ISD256CS2A-8T
512 MB	AP-ISD512CS2A-8T
1 GB	AP-ISD01GCS2A-8T
2 GB	AP-ISD02GCS2A-8T
4 GB	AP-ISD04GCS4A-8T
8 GB	AP-ISD08GCD4A-8T
16 GB	AP-ISD16GCD4A-8T
32 GB	AP-ISD32GCD4A-8T

5.2.2 Extended Temperature

Capacity	AP/N
256 MB	AP-ISD256IS2B-8T
512 MB	AP-ISD512IS2B-8T
1 GB	AP-ISD01GIS2B-8T
2 GB	AP-ISD02GIS2B-8T
4 GB	AP-ISD04GIS4B-8T
8 GB	AP-ISD08GID4B-8T
16 GB	AP-ISD16GID4B-8T
32 GB	AP-ISD32GID4B-8T

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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Revision History

Revision	Description	Date
1.0	Official release	02/25/2015
1.1	Revised durability specifications	04/21/2016

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Global Presence

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